Session 2 Overview: *RF Frequency Synthesis Techniques*

RF SUBCOMMITTEE

Session Chair: *Ahmad Mirzaei, Broadcom, Irvine, CA*

Session Co-Chair: *Hyunchol Shin, Kwangwoon University, Seoul, Korea*

Frequency generation and synthesis circuits are ubiquitous building blocks in communication, sensing, and imaging systems. This session covers the latest advances in frequency synthesizers and VCOs in GHz and THz frequency ranges. The session begins with a CMOS frequency synthesizer operating above 0.5THz and a 28GHz coupled PLL for mm-Wave 5G applications. The session also presents two GHz-range PLLs, which include a PLL-DLL cascaded structure operating over a wide bandwidth and achieving low phase noise and a high-performance BiCMOS fractional-N synthesizer for backhaul applications. Two VCOs are presented next. The first VCO is a low-power complementary VCO with a low flicker noise corner. This is followed by a 190GHz VCO with very wide tuning range and a time-interleaved ring VCO with a low $1/f^3$ noise corner. The last two papers describe an injection-locked frequency-locked loop with a self-calibrated locking algorithm and a 2GHz 244fs-resolution digital-to-time converter.

1:30 PM

2.1 An Integrated 0.56THz Frequency Synthesizer with 21GHz Locking Range and -74dBc/Hz Phase Noise at 1MHz Offset in 65nm CMOS

Y. Zhao, University of California, Los Angeles, CA

In Paper 2.1, UCLA, JPL and TSMC present the first integrated synthesizer realized in silicon IC operating above 0.5THz. The 65nm CMOS 0.56THz frequency synthesizer has a 21GHz locking range and -74dBc/Hz phase noise at 1MHz offset.

2:00 PM

2.2 A Scalable 28GHz Coupled-PLL in 65nm CMOS with Single-Wire Synchronization for Large-Scale 5G mm-Wave Arrays

A. Agrawal, Oregon State University, Corvallis, OR

In Paper 2.2, Oregon State presents a scalable, single-wire synchronization architecture and circuits for mm-Wave arrays that preserve the simplicity of daisy-chained LO distribution, compensate for phase offset due to interconnect, and provide phase noise improvement with an increasing number of PLLs. Measurements on a scalable 28GHz prototype demonstrate a 21% improvement in *rms* jitter and a 3.4dB improvement in phase noise at a 10MHz offset when coupling 28GHz PLLs across three different ICs.

2:30 PM

2.3 A 4.2μs-Settling-Time 3rd-Order 2.1GHz Phase-Noise-Rejection PLL Using a Cascaded Time-Amplified Clock-Skew Sub-Sampling DLL

Z. Huang, Hong Kong University of Science and Technology, Hong Kong, China

In Paper 2.3, HKUST presents a 2.1GHz PLL in 65nm CMOS employing a Type-II PLL cascaded with a time-amplified clock-skew sub-sampling DLL to achieve a 40MHz-bandwidth and 3rd-order phase-noise rejection of VCO phase noise without degrading stability and bandwidth.

 978-1-4673-9467-3/16/$31.00 ©2016 IEEE

3:15 PM

2.4 A 2-to-16GHz BiCMOS ΔΣ Fractional-N PLL Synthesizer with Integrated VCOs and Frequency Doubler for Wireless Backhaul Applications

T. Copani, STMicroelectronics, Catania, Italy

In Paper 2.4, STMicroelectronics presents a 2-to-16GHz BiCMOS ΔΣ fractional-N PLL synthesizer with integrated VCOs and frequency doubler for wireless backhaul applications.

3:45 PM

2.5 A Complementary VCO for IoE that Achieves a 195dBc/Hz FOM and Flicker Noise Corner of 200kHz

D. Murphy, Broadcom, Irvine, CA

In Paper 2.5, Broadcom presents a 4.7-to-5.4GHz complementary VCO with a 195dBc/Hz FoM and a flicker noise corner of 200kHz, which is suitable for ultra-low-power IoE applications.

4:00 PM

2.6 A 190.5GHz Mode-Switching VCO with 20.7% Continuous Tuning Range and Maximum Power of -2.1dBm in 0.13µm BiCMOS

R. Kananizadeh, University of California, Davis, CA

In Paper 2.6, University of California, Davis, describes a 190.5GHz mode-switching VCO with a 20.7% continuous tuning-range and the maximum power of -2.1dBm in 0.13µm BiCMOS.

4:15 PM

2.7 A 0.003mm² 1.7-to-3.5GHz Dual-Mode Time-Interleaved Ring-VCO Achieving 90-to-150kHz 1/f³ Phase-Noise Corner

J. Yin, University of Macau, Macau, China

In Paper 2.7, University of Macau, University of Pavia and Instituto Superior Tecnico present a 1.7-to-3.5GHz dual-mode time-interleaved ring-VCO that achieves 90-to-150kHz 1/f³ phase noise corner

4:30 PM

2.8 A Mixed-Mode Injection Frequency-Locked Loop for Self-Calibration of Injection Locking Range and Phase Noise in 0.13µm CMOS

D. Shin, Virginia Tech, Blacksburg, VA

In Paper 2.8, Virginia Tech presents a mixed-mode injection frequency-locked loop with a self-calibration of injection locking range and phase noise in 0.13µm CMOS.

4:45 PM

2.9 A 2GHz 244fs-Resolution 1.2ps-Peak-INL Edge-Interpolator-Based Digital-to-Time Converter in 28nm CMOS

S. Sievert, Intel, Neubiberg, Germany

In Paper 2.9, Intel and Technical University of Munich present a 2GHz, 244fs resolution, 1.2ps peak INL edge-interpolator-based digital-to-time converter in 28nm CMOS.

2.1 An Integrated 0.56THz Frequency Synthesizer with 21GHz Locking Range and -74dBc/Hz Phase Noise at 1MHz Offset in 65nm CMOS

Yan Zhao[1], Zuow-Zun Chen[1], Gabriel Virbila[1], Yinuo Xu[1], Richard Al Hadi[1], Yanghyo Kim[1,2], Adrian Tang[1,2], Theodore Reck[2], Huan-Neng Chen[3], Chewnpu Jou[3], Fu-Lung Hsueh[3], Mau-Chung Frank Chang[1,4]

[1]University of California, Los Angeles, CA,
[2]Jet Propulsion Laboratory, Pasadena, CA, [3]TSMC, Hsinchu, Taiwan,
[4]National Chiao Tung University, Hsinchu, Taiwan

Spectra from 0.5 to 0.6THz play critical roles in planetary science, astrophysics and radio-astronomy as various chemical species including water, nitrates (NO_2, N_2O, NH_3) and organics (CH_4 and HCN) can either absorb or reflect radiation in this frequency regime. Accordingly, NASA and ESA have developed a wide range of spectroscopic sounding instruments to investigate our solar system. Current LO chains for spectroscopic receivers are implemented with discrete III-V devices and heavy waveguide assemblies. For instance, the 600GHz NASA PISSARRO spectrometer for Europa begins with a 33GHz PLL, tripled to 100GHz, doubled to 200GHz, and then tripled again to 600GHz via multiple waveguides. This LO chain occupies over 3000cm^3, weighs 2.5kg, and consumes 11.5W of DC power.

Frequency synthesizers around 0.3THz demonstrated in SiGe HBTs confirmed the potential of implementing a terahertz LO in IC technologies [1,2]. It would be beneficial to further develop frequency synthesizers at the scientifically important 0.5-to-0.6THz in mainstream CMOS technologies with larger integration and lower power than that of SiGe HBT counterparts. Although VCOs/multipliers [3-6] have been developed at these frequencies, the realization of wide-bandwidth and low-phase-noise synthesizers remains challenging due to the following obstacles: (a) the use of varactors or other passives for frequency tuning radically lowers the tank quality and inhibits oscillation; (b) there is no proven injection-locked frequency divider (ILFD) that can operate beyond 0.2THz with a sufficiently wide frequency locking range. To date, no silicon based synthesizer has been reported beyond 0.32THz.

We report realization of a 0.54-to-0.56THz synthesizer (Fig. 2.1.1) in a standard 65nm CMOS technology. Its front-end is composed of a primary triple-push Colpitts oscillator (P-TPCO), an auxiliary TPCO (A-TPCO), a single-ended Colpitts oscillator (SECO), a 1st ILFD, and a 2nd wide band ILFD, followed by a divide-by-16 static-frequency-divider chain. The P-TPCO delivers its 3rd harmonic for the intended LO at 0.56THz, while the A-TPCO and the subsequent Colpitts oscillator (CO) bridge it to the 1st IFDL. It is nevertheless impossible to exploit ILFD directly at 0.56THz. We thus use 1st ILFD to divide the P-TPCO 186.7GHz fundamental frequency to 93.3GHz, and use the 2nd ILFD and the subsequent divider chain for further divisions in the PLL feedback loop. To eliminate noise from the charge pump and multi-modulus dividers (MMD), the PLL uses a sub-sampled phase detector (SSPD) [7], followed by a Gm cell, which converts the phase error to current that charges an off-chip loop filter and supplies TPCO control voltage, V_{CTL}. An auxiliary frequency-locked loop with a conventional MMD, a phase-frequency detector (PFD) and a charge pump (CP) conducts an automatic frequency search before enabling the SSPD to lock to the precise phase. A 3-wire digital serial peripheral interface (SPI) is used to control the tuning-knob DACs throughout the synthesizer.

Both P- and A-TPCOs are constructed and synchronized using similar concepts from [5]. They are formed with three-CO branches joined via their drain inductors, L_D, to convey the 3rd harmonic at the common push node (CPN) (Fig. 2.1.2). When operated in the intended mode, the fundamental currents among three branches shift by 120° from each other, producing an in-phase 3rd-harmonic output at the CPN. The A-TPCO is used to isolate the P-TPCO from the following stages and runs at 180° out-of-phase via direct current coupling, in which a common-gate bias node, V_{GG}, is shared by two TPCO-coupling branches through an AC-grounded 1/4λ transmission line. A CO further isolates the P-TPCO from unbalancing caused by the 1st ILFD loading and carries the P-TPCO fundamental frequency to the injection port of the 1st ILFD. The 2nd ILFD is incorporated with a digitally controlled artificial-dielectric (DiCAD) tuning elements [7] to program its operating frequency from 41.5 to 52.5GHz.

Three key contributions enable desired locking range through all front-end stages (Fig. 2.1.2). First, band-selection switches are incorporated with source inductors, L_S, of all COs and tank inductor, L_T, of the 1st ILFD. Those switches controlled by V_{SW1} and V_{SW2}, respectively, can truncate L_S and L_T for selecting multiple operation bands. Second, major front-end blocks, including the P-TPCO, the A-TPCO, the SECO and the 1st ILFD, are tuned simultaneously by a common control voltage, V_{CTL}, which dynamically aligns the 1st ILFD and the operating frequency of the oscillators over the entire V_{CTL} range. Additionally, to avoid inherent losses of varactors at THz frequencies, we instead apply V_{CTL} at device bulk nodes. Third, the 1st ILFD is configured as a cross-coupled oscillator with two separate injection mechanisms: one via the NMOS switch Q_5 and the other via the center tap of L_T to enhance its injection locking sensitivity.

We adopted free-space measurement to simplify testing of the 65nm-CMOS prototype with an on-chip antenna. To radiate THz signals more effectively, the synthesizer chip is assembled with a silicon hyper-hemispherical lens on the backside of the substrate. The testing setup is shown in Fig. 2.1.3. The radiated THz signal spectrum is validated by using a spectrum analyzer that receives a down-converted THz signal at IF from a VDI subharmonic mixer with a WR1.5 horn. The radiated power was characterized with a calibrated pyroelectric THz radiometer. As shown in Fig. 2.1.4, the locked output frequencies span from 538.67 to 559.89GHz with tunable reference signals from 103.9 to 108MHz, covering 6 continuous channels with different settings on DiCAD and band-selection switches Q_2 and Q_5. The measured radiated power varies from -30 to -27dBm over the 21.22GHz locking band (the simulated antenna efficiency is 50%). InP HEMT amplifiers [8] may be an avenue to further increase the LO power in future THz systems. In the above measurements, IR radiation is blocked and the fundamental leakage is verified to be insignificant (at least 10dB lower than the 3rd harmonic) using the techniques of [5]. The phase noise at 559.89GHz is characterized in Fig. 2.1.5 as -71, -74 and -85dBc/Hz at 100kHz, 1MHz and 10MHz offset, respectively, with a high quality 108MHz crystal reference. Limited visibility of the measured phase noise skirt is a result of the high free-space, mixer and antenna losses, providing a signal of less than 30dB above the spectrum analyzer noise floor. The synthesizer prototype consumes 172mW in total under a separate 1V and 2.5V power supplies (1mA/2.5V for SPI and one DAC). Its performance is compared with that of prior arts in Fig. 2.1.6 and is shown to be the only silicon-IC frequency synthesizer operating beyond 0.5THz. The die occupies 1.8x1.55mm^2 area (Fig. 2.1.7). Compared with MMIC synthesizers in existing NASA THz instruments (limited <100GHz), our CMOS frequency synthesizer can considerably reduce weight, volume and power as no III/V multiplication stages needed.

Acknowledgements:
This work was supported by the US Air Force Office of Scientific Research under Grant No. FA9550-12-1-0181 and in part by the US Army Research Office under Grant No. W911NF-14-1-0665. The authors are grateful to Alcatera LLC for technical consultation.

References:
[1] P.-Y. Chiang et al., "A 300GHz Frequency Synthesizer with 7.9% Locking Range in 90nm SiGe BiCMOS," *ISSCC Dig. Tech. Papers*, pp. 260-261, Feb. 2014.
[2] R. Han et al., "A 320GHz Phase-Locked Transmitter with 3.3mW Radiated Power and 22.5dBm EIRP for Heterodyne THz Imaging Systems," *ISSCC Dig. Tech. Papers*, pp. 1-3, Feb. 2015.
[3] W. Steyaert and P. Reynaert, "A 0.54 THz Signal Generator in 40 nm Bulk CMOS With 22 GHz Tuning Range and Integrated Planar Antenna," *IEEE J. Solid-State Circuits*, vol. 49, no. 7, pp.1617–1626, July 2014.
[4] U. Pfeiffer et al., "A 0.53THz Reconfigurable Source Array with up to 1mW Radiated Power for Terahertz Imaging Applications in 0.13μm SiGe BiCMOS," *ISSCC Dig. Tech. Papers*, pp. 256-257, Feb. 2014.
[5] Y. Zhao et al., "A 0.54-0.55 THz 2x4 Coherent Source Array with EIRP of 24.4 dBm in 65nm CMOS Technology," *IEEE Int. Microwave Symp.,* May 2015.
[6] T. Chi et al., "A Multi-Phase Sub-Harmonic Injection Locking Technique for Bandwidth Extension in Silicon-Based THz Signal Generation", *IEEE J. Solid-State Circuits*, vol. 50, no. 8, pp. 1861–1873, Aug. 2015.
[7] Z.-Z. Chen et al., "A Wide-band 65nm CMOS 28-34 GHz Synthesizer Module Enabling Low Power Heterodyne Spectrometers for Planetary Exploration," *IEEE Int. Microwave Symp.*, May 2015.
[8] V. Radisic et al., "InP HBT Transferred Substrate Amplifiers Operating to 600 GHz," *IEEE Int. Microwave Symp.*, May 2015.

 978-1-4673-9467-3/16/$31.00 ©2016 IEEE

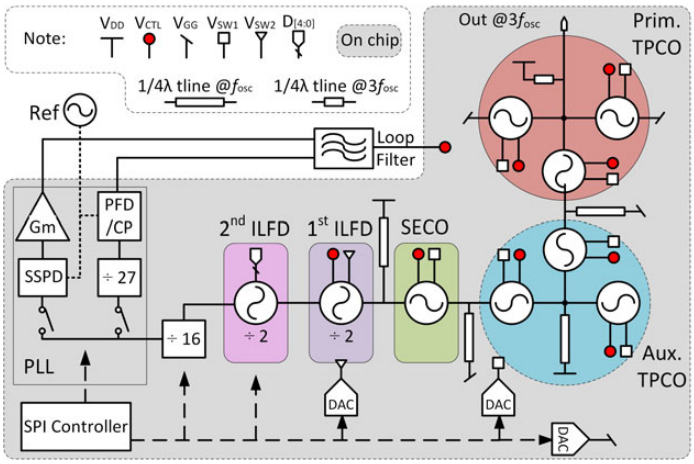


Figure 2.1.1: 0.56THz-frequency-synthesizer block diagram (Note: the red circle pins for VCTL are all connected, indicating that frequency control pins from 2 TPCOs, 1 SECO and the 1st ILFD are tuned simultaneously.)

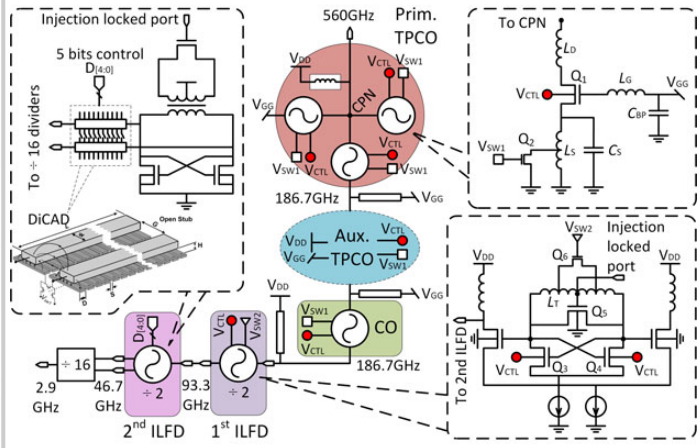


Figure 2.1.2: Schematics of front-end blocks with three key contributions to maximize achievable locking bandwidth. First, band selection switches Q2 and Q5; Second, simultaneously tuned VCTL applied on both oscillators and 1st ILFD; Third, the 1st ILFD is injection-locked at two pins.

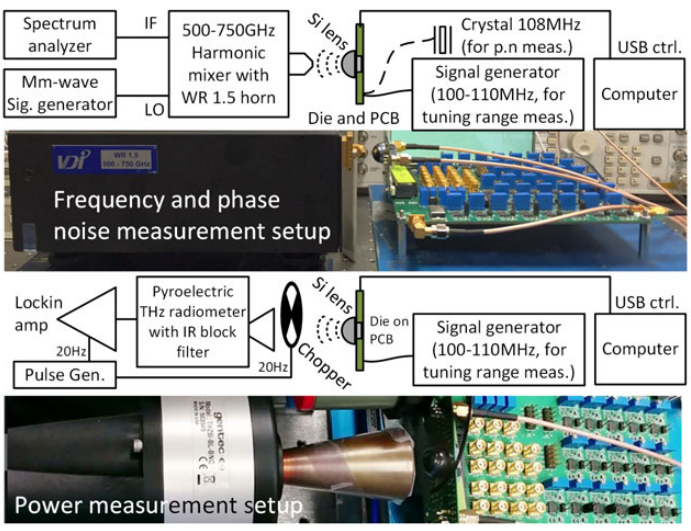
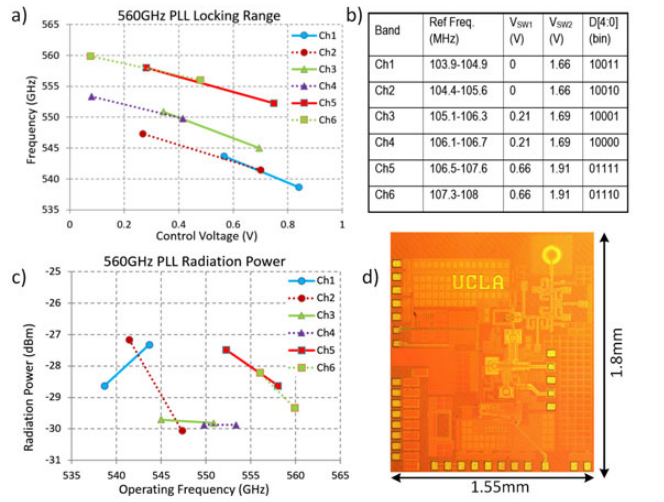
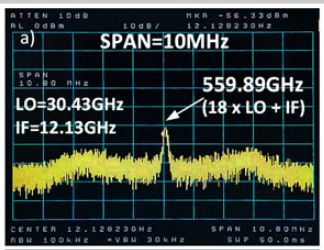


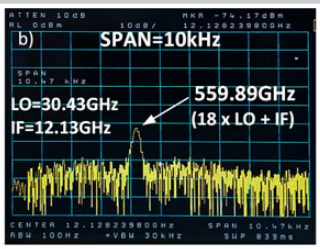
Figure 2.1.3: Characterization setup for spectrum and power measurement.

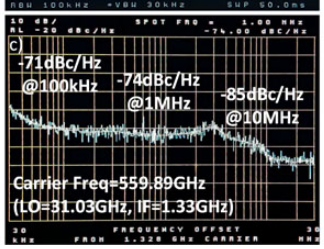


Band	Ref Freq. (MHz)	V_{SW1} (V)	V_{SW2} (V)	D[4:0] (bin)
Ch1	103.9-104.9	0	1.66	10011
Ch2	104.4-105.6	0	1.66	10010
Ch3	105.1-106.3	0.21	1.69	10001
Ch4	106.1-106.7	0.21	1.69	10000
Ch5	106.5-107.6	0.66	1.91	01111
Ch6	107.3-108	0.66	1.91	01110

Figure 2.1.4: Measurement results: a) Freq. locking range vs ref. freq.; b) settings of switch voltages and DiCAD control bits; c) Radiation power vs freq.; d) Die micrograph with an on-chip antenna.







d)

Freq. Offset	108MHz Crystal Phase Noise	560GHz PLL Phase Noise
100kHz	-164.7dBc/Hz	-71dBc/Hz
1MHz	-168.6dBc/Hz	-74dBc/Hz
10MHz	-168dBc/Hz	-85dBc/Hz

Figure 2.1.5: Phase noise measurement results: 559.89GHz locked tone stabilized by 108MHz crystal in a) 10MHz and b) 10kHz spans; c) and d) Measured phase noise from 30kHz to 30MHz. Note: the crystal phase noise data is provided from product datasheet.

	Configuration	Max. Freq. (GHz)	Tech. (f_{max})	Ph. Noise (dBc/Hz @1MHz)	DC Power (mW)
[1] ISSCC 2014	PLL + VCO	280.0-303.4	SiGe (315GHz)	-82.5	376
[2] ISSCC 2015	PLL + Osc. array	317	SiGe (280GHz)	-79	610
[3] JSSC 2014	VCO + tripler	539.6-561.5	40nm CMOS	Free running	16.8
[4] ISSCC 2014	Non coherent osc. array	519-536 ††	SiGe (500GHz)	Free running	2500
[5] IMS 2015	Coherent VCO array	540-550	65nm CMOS (240GHz)	Free running	1300
[6] JSSC 2015	Injection lock. Osc. chain	485.1-510.7	SiGe (350GHz)	Free running	425
This work	**PLL + VCO**	**538.7-559.9**	**65nm CMOS (240GHz)**	**-74**	**172**

†† Tuned by varying power supply

Figure 2.1.6: Performance comparisons with state-of-the-art works.

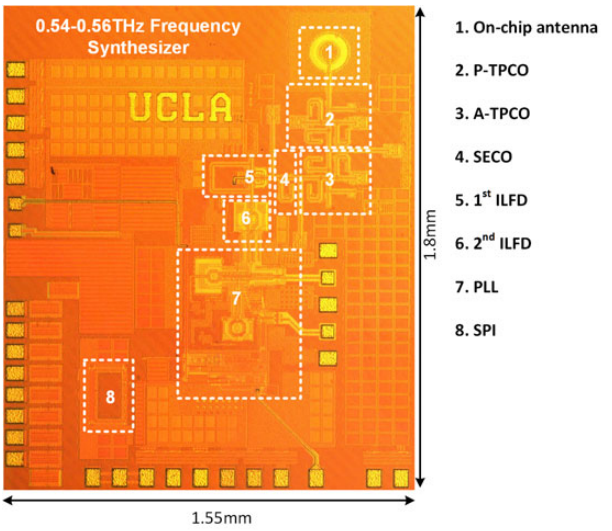


Figure 2.1.7: Die micrograph with floor plan description (on-chip antenna is only for testing purpose to avoid using THz probes).

978-1-4673-9467-3/16/$31.00 ©2016 IEEE

2.2 A Scalable 28GHz Coupled-PLL in 65nm CMOS with Single-Wire Synchronization for Large-Scale 5G mm-Wave Arrays

Abhishek Agrawal, Arun Natarajan

Oregon State University, Corvallis, OR

Demonstrations of mm-Wave arrays with >50 elements in silicon has led to an interest in large-scale mm-Wave MIMO arrays for 5G networks, which promise substantial improvements in network capacity [1,2]. Practical considerations result in such arrays being developed with a tiled approach, where *N* unit cells with *M* elements each are tiled to achieve large MIMO/phased arrays with *NM* elements [2]. Achieving stringent phase-noise specifications and scalable LO distribution to maintain phase coherence across different unit cell ICs/PCBs are a critical challenge. In this paper, we demonstrate a scalable, single-wire-synchronization architecture and circuits for mm-Wave arrays that preserve the simplicity of daisy-chained LO distribution, compensate for phase offset due to interconnects, and provide phase-noise improvement with increasing number of PLLs [3]. Measurements on a scalable 28GHz prototype demonstrate a 21% improvement in rms jitter and a 3.4dB improvement in phase noise at 10MHz offset when coupling 28GHz PLLs across three different ICs.

LO or reference distribution to PLLs on unit-cell ICs using a symmetric H-tree distribution network presents scalability challenges. While daisy-chained LO/reference distribution networks can provide a scalable approach, the reference-signal phase noise is degraded as it is transferred along the daisy-chain [2]. Additionally, the phase offset between elements must be calibrated due to unidirectional reference signaling. Importantly, both *H*-tree and daisy-chain schemes do not provide any performance benefits as the number of ICs (PLLs) operating in the array increase. Bidirectional coupling between PLLs as shown in Fig. 2.2.1 can eliminate phase offset variations and provide phase-noise improvement within the coupling bandwidth but this approach doubles the number of IO pins and increases the layout complexity. In this paper, we demonstrate a single-wire coupled-PLL approach (Fig. 2.2.1) that can couple two PLLs with only one interconnect between them. This approach is extended to a scalable synchronization scheme with dual-input PLLs, where the PLL on $Tile_K$ is coupled with the PLLs on $Tile_{K-1}$ and $Tile_{K+1}$ without adding any board-level overhead when compared to daisy-chained reference distribution. It can be shown that for dual-input type-II PLLs, a steady-state solution exists when a reference signal is present (shown for three PLLs in Fig. 2.2.1), albeit with a phase offset between the LO signals on multiple ICs. However, this static offset can be undesirable for a PLL and must be minimized. In comparison with coupled injection-locked oscillator-based arrays [4], the proposed architecture operates with a reference, and the type-II approach does not require static phase offsets for phase locking.

Figure 2.2.2 shows the schematic of the dual-input 28GHz PLL that targets the single-wire bidirectional PLL-coupling concept outlined in Fig. 2.2.1. The LO chain consists of a 25.3-to-30.4GHz LC-VCO that drives a low-power frequency-tunable injection-locked divide-by-two. Following this, a CML divide-by-four generates ~3.5GHz signal and drives PD1 and PD2 as well as the output buffers, *BUF1* and *BUF2*, that are matched to 50Ω. A type-II PLL with dual differential ~3.5GHz mixer-PD drives the differential VCO varactors. Critical challenges include: (a) achieving bidirectional coupling while distinguishing between the VCO signal and the reference signal at each common IO port and (b) accommodating interconnect phase shifts to achieve low static phase offset between the inputs to the phase detectors. The latter challenge is addressed by incorporating >2π variable phase shift in the path between the output driver ($BUF1_K$ *or* $BUF2_K$) on $Tile_K$ and the input to the phase detector ($PD2_{K-1}$ or $PD1_{K+1}$), respectively, on the adjacent PLL. First, output buffers, *BUF1* and *BUF2,* can select any one of quadrature phases from the CML dividers providing 90° coarse phase shift. Second, as detailed in the following, the IO-coupling block also provides variable-phase-shift capability to compensate for interconnect phase shifts. A low loop-bandwidth varies phase shift in the IO-coupling block to ensure a quadrature phase difference between the mixer-PD input signals at 3.5GHz, which is equivalent to $2m\pi$ phase offset at 28GHz.

Figure 2.2.3 shows the schematic of the ~3.5GHz IO-coupling block that (a) senses the input signal incident on *P1* and (b) provides a variable phase shift for signals travelling from *P2* to *P1*. The block is based on a 3dB quadrature coupler, where the coupled and through ports are terminated with high impedances. As shown in Fig. 2.2.3, the signals at *Thru* and *Cpl* are in quadrature with *Cpl* leading *Thru* for the input at *P1* and *Thru* leading *Cpl* for the input at *P2*. Therefore, a polyphase filter that combines the outputs at *Thru* and *Cpl* can reject signals from *P2* while only selecting signals from *P1* as shown in Fig. 2.2.3. In this work, a lumped 3.5GHz hybrid coupler is implemented using a transformer and MIM capacitors. The voltages at *Thru* and *Cpl* are sensed using transconductances ($G_{M1,2}$). Baluns at the output of $G_{M,1,2}$ create differential signals that drive a programmable *RC* polyphase filter. A variable capacitance, C_P, is included in the resonator of the G_{M12} to provide a variable phase shift. Figure 2.2.3 shows the simulated gain performance as well as the measured phase shift across quadrature polyphase outputs and capacitor, C_P, settings. The IO-coupling topology can further be viewed as a reflection-type phase shifter between P2 (buffer output) and P1 (chip input/output). A variable capacitance, C_{RTPS}, consisting of a digital coarse step and analog varactor, is included at *Thru* and *Cpl*, creating a variable phase shift between *P2* to *P1* without affecting the incident signal at *P1* that is sensed by G_{M1} and G_{M2}. The varactor is controlled by the DLL, which minimizes phase offset between PD inputs. Simulated insertion losses with and without the variable C_{RTPS} between *P1* and *P2* are 2.7-to-4.8dB and 1.6dB, respectively. The output buffer is matched to 50Ω and consumes ~3.5mA to generate a 0dBm output.

The dual-input 28GHz PLL is implemented in a 65nm CMOS process with 3.4mm-thick top-metal layer and occupies 1.5mm×1.6mm (including test circuits that occupy ~25% of the area). The IC is packaged using a Rogers 4350 board with chip-on-board packaging. The VCO and the PLL phase noise performance is characterized using an R&S FSUP26 signal analyzer. The measured VCO tuning range and the open-loop phase noise of the VCO with the injection locked divider and the CML dividers are shown in Fig. 2.2.4. The VCO achieves 18% tuning range at 27.5GHz, with an optimum FOM of ~181dB while consuming 3.9mW. The single PLL and the cascaded/coupled PLL performance are characterized at the divided 3.5GHz output. The stand-alone VCO and the divider chain achieve a phase noise of -135dBc/Hz at 10MHz offset for 3.5GHz output. Figure 2.2.5 shows the 28GHz PLL phase noise for the stand-alone PLL with the reference loop bandwidth of ~2MHz and a low-noise reference provided by an Anritsu MG3694C. In subsequent measurements, two and three PLLs are coupled with the setup shown in Fig. 2.2.5 and Fig. 2.2.6. Following a coarse phase calibration and DLL activation, the three PLLs are able to stay in lock throughout the varactor tuning range (~100MHz in each band). Transfer functions with respect to the reference input are measured to characterize loop bandwidths. Measured phase noise for a constant loop bandwidth (~2MHz) with two and three PLLs coupled are shown in Fig. 2.2.5 demonstrating ~3dB-to-5dB phase noise improvement. Measured phase noise with three PLLs in a cascaded and coupled mode is shown in Fig. 2.2.6 while the loop settings were calibrated to match the transfer function from the reference input to the output. When coupling is enabled, a phase noise improvement is observed within the coupling bandwidth (~40MHz) with lower PLL rms jitter of 104fs. Notably, PLL FOM [5] (including all buffer and G_M-cell power consumption) improves with increasing number of elements. The die micrograph is shown in Fig. 2.2.7.

Acknowledgements:
This work is supported by the DARPA Arrays at Commercial Timescales Program. We thank Rohde & Schwarz for equipment support.

References:
[1] A. Swindlehurst et al., "Millimeter-Wave Massive MIMO: The Next Wireless Revolution," *IEEE Communications Magazine,* vol. 52, no. 9, pp. 56-62, Sept. 2014.
[2] X. Gu et al., "A Compact 4-chip Package with 64 Embedded Dual-Polarization Antennas for W-band Phased-Array transceivers," *IEEE Electronic Components and Technology Conf.,* pp. 1272-1277, May 2014.
[3] H.-C. Chang, "Analysis of Coupled Phase-Locked Loops with Independent Oscillators for Beam Control Active Phased Arrays," *IEEE Trans. Microwave Theory and Techniques,* vol. 52, no. 3, pp. 1059-1066, Mar. 2004.
[4] P. Liao and R. York, "A new Phase-Shifterless Beam-Scanning Technique using Arrays of Coupled Oscillators," *IEEE Trans. on Microwave Theory and Techniques*, vol. 41, no. 10, pp. 1810-1815, Oct. 1993.
[5] X. Gao et al., "Jitter Analysis and a Benchmarking Figure-of-Merit for Phase-Locked Loops," *IEEE Trans. Circuits and Systems-II*, vol. 56, no. 2, pp. 117-121, Feb. 2009.

 978-1-4673-9467-3/16/$31.00 ©2016 IEEE

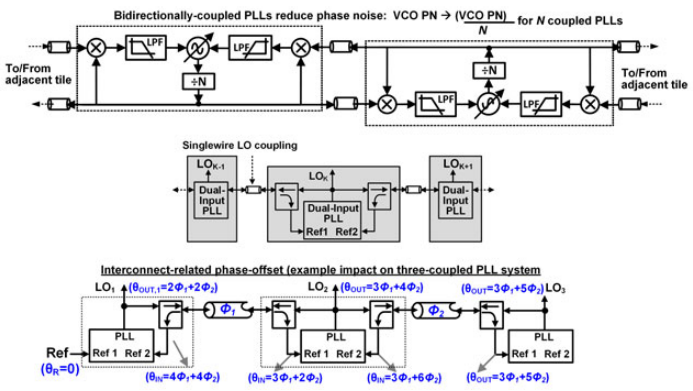


Figure 2.2.1: Proposed scalable, single-wire approach for coupling-PLLs across multiple ICs in a large-scale mm-Wave array, leading to reduction in phase noise and jitter.

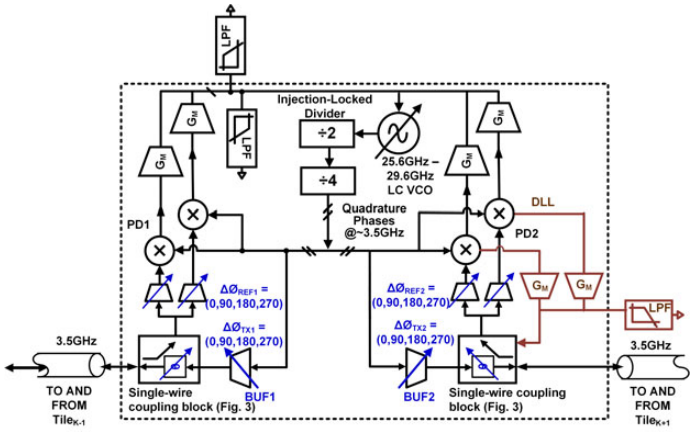


Figure 2.2.2: Schematic of a 28GHz dual-input PLL targeting scalable synchronization. A DLL with low loop bandwidth senses the phase offset and ensures quadrature input to mixer-PD.

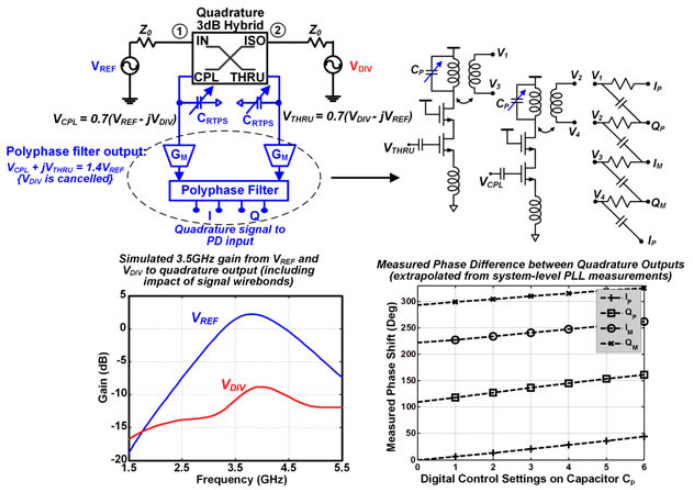


Figure 2.2.3: Schematic and simulated/measured performance of the 3.5GHz bidirectional IO coupling block.

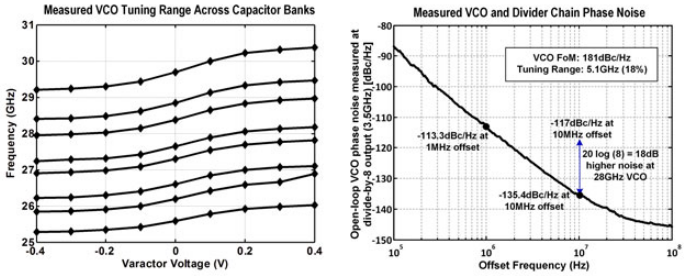


Figure 2.2.4: Measured 28GHz-VCO tuning range across switched capacitor banks and measured open-loop VCO phase noise.

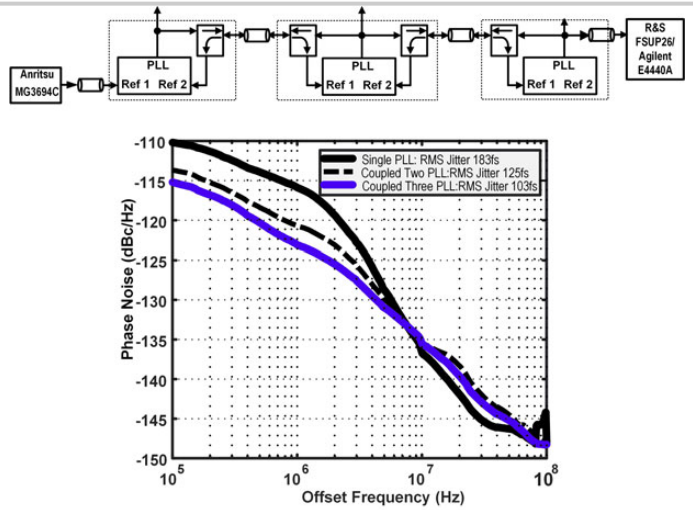
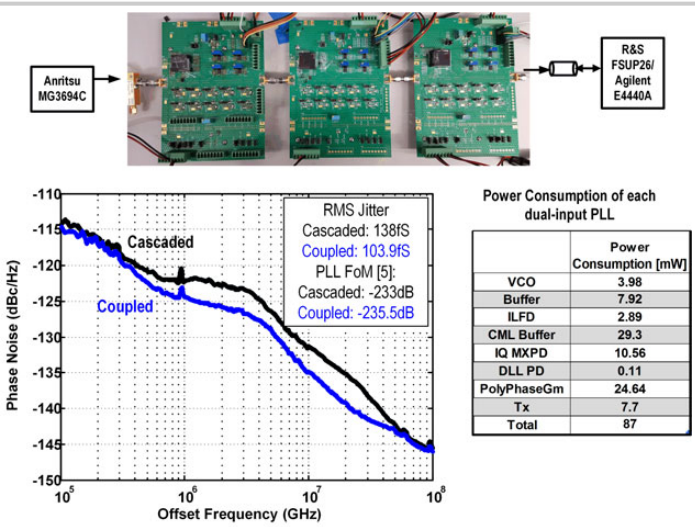


Figure 2.2.5: Measured 28GHz-PLL phase noise for a single PLL and with two and three PLLs coupled with a constant reference loop bandwidth (measurements at 3.5GHz divided output).



	Power Consumption [mW]
VCO	3.98
Buffer	7.92
ILFD	2.89
CML Buffer	29.3
IQ MXPD	10.56
DLL PD	0.11
PolyPhaseGm	24.64
Tx	7.7
Total	87

Figure 2.2.6: Measured performance of three PLLs. The PLLs are placed in cascaded or coupled mode based on the PD and output buffer settings.

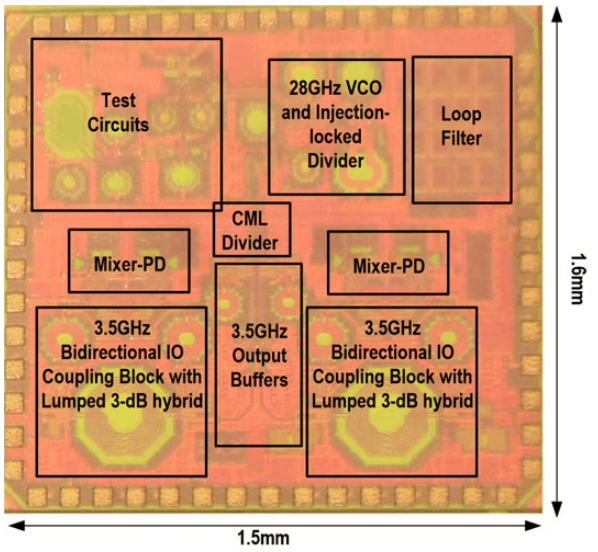


Figure 2.2.7: Die micrograph of the single-wire scalable 28GHz coupled PLL.

978-1-4673-9467-3/16/$31.00 ©2016 IEEE

2.3 A 4.2μs-Settling-Time 3rd-Order 2.1GHz Phase-Noise-Rejection PLL Using a Cascaded Time-Amplified Clock-Skew Sub-Sampling DLL

Zhiqiang Huang[1], Bingwei Jiang[1], Lianming Li[2], Howard Cam Luong[1]

[1]Hong Kong University of Science and Technology, Hong Kong, China, [2]Southeast University, Nanjing, China

Ring-VCO-based PLLs are popular because of their compact chip area and wide tuning range compared with LC-VCO-based PLLs. However, they typically have higher jitter and larger frequency drift due to high sensitivity to PVT variations. Several PLL architectures were proposed to reject the phase noise and reduce the frequency drift [1,2]. However, due to an architecture-level limitation, these phase-noise-rejection PLLs inevitably degrade the settling time. To suppress large phase noise (PN) and supply sensitivity, a Type-III PLL was proposed to provide a large low-frequency loop gain by using a 3rd-order feedback loop [1]. However, high-order feedback loop degrades stability and requires low-frequency compensation zero, which needs a large loop filter and reduces the PN suppression bandwidth. To suppress the phase noise over a wide frequency offset, injection-locked (IL) PLL was proposed by injecting a clean reference into a noisy VCO [2]. But a sub-harmonic injection into a ring-VCO requires a pulse generator, which enhances harmonics but generates large reference spurs. Besides, a race condition between the injection-locking path and the PLL path weakens the locking strength and prolongs settling time by 5 times [2]. In order to reject the phase noise and to minimize supply sensitivity and frequency drift of ring-VCO-based PLLs without compromising other parameters, this paper proposes a 3rd-order PLL employing a cascaded time-amplified clock-skew-sub-sampling DLL, measuring a 4.2μs settling time, 1.05ps integrated jitter, and -113dBc/Hz in-band phase noise with a 3.84mW power consumption at a 2.1GHz output frequency.

Figure 2.3.1 (top left) illustrates the conceptual model of the proposed cascaded PLL. A sub-sampling DLL consists a high-frequency noisy source driving a voltage-controlled delay line (VCDL) and a sub-sampling phase detector (PD) sensing the residual phase error ϕ_e at the input to the PD. The phase error is fed back through a 1st-order loop filter to control and adjust the VCDL delay suppressing the phase noise of the noisy input source. As such, the sub-sampling DLL becomes a 1st-order feedback loop and the phase transfer function from the noise source ϕ_{n1} to the output ϕ_{n2} exhibits a high-pass response while that from the reference input ϕ_{REF} to the output ϕ_{n2} is a low-pass function. Because the sub-sampling DLL is a 1st-order feedback loop with a large phase margin, it is capable of rejecting the phase noise of a noisy input source over a wide frequency range as in IL-PLLs [2] and in Type-I PLLs [3].

For the sub-sampling DLL to lock with a small phase error, the frequency of the noisy input source should be an integral multiple of the reference frequency. As a result, the cascaded PLL uses an integer-N PLL as noisy source (Fig. 2.3.1 top right) and is cascaded with a 1st-order sub-sampling DLL to provide wideband high-pass phase-noise rejection to the output of the integer-N PLL. With the output frequency of the cascaded PLL still being an integral multiple of the reference frequency, it can be further cascaded (bottom of Fig. 2.3.1) with another sub-sampling DLL for even more phase-noise suppression. In this way, it becomes an n-stage cascaded PLL consisting of one integer-N PLL as the first stage followed by (n-1) sub-sampling DLLs. Compared with conventional PLLs, the n-stage cascaded PLL has an (n-1) higher order of phase-noise rejection without degrading phase margin because the sub-sampling DLLs are cascaded without forming any single high-order feedback loop.

Figure 2.3.2 shows the block diagram of the proposed 2-stage cascaded PLL. It consists of an integer-N Type-II PLL for frequency acquisition and phase locking and a cascaded clock-skew sub-sampling DLL to provide 3rd-order phase locking. The Type-II PLL consists of a ring oscillator (RO) operating from 1.1 to 2.1GHz and a frequency divider with a division ratio from 16 to 31 and is locked to a reference frequency by a phase-frequency detector (PFD), a charge-pump (CP), and a loop filter. Because of a low loop gain and a narrow loop bandwidth for rejecting the RO phase noise, the Type-II PLL has high output phase noise ϕ_{n1}. By cascading the Type-II PLL with a wideband 1st-order clock-skew sub-sampling DLL as shown in Fig. 2.3.2, the proposed cascaded PLL provides a wideband 3rd-order phase noise rejection at the first-stage PLL output. Instead of a conventional sub-sampling PD, the proposed clock-skew sub-sampling DLL employs a clock-skew sub-sampling PD, which consists of a VCDL with a gain of 100ps/V, a clock-skew sub-sampling PD with a re-timer to detect the VCDL output phase error, and a charge pump followed by a capacitor as a loop filter to integrate the phase error and adjust the VCDL delay. This architecture suppresses the output phase noise ϕ_{n1} of the Type-II PLL by $1+ K_{VCDL}H_{LF}(s)$.

Compared with a conventional sub-sampling PD [4], the clock-skew-sub-sampling PD has a much wider detection range. As shown in Fig. 2.3.3, the conventional sub-sampling PD detects the output phase by sampling the VCO output using a MOSFET switch, and the phase error is converted into sampled voltage V_{samp} to control the charge pump current. The PLL can work correctly with a phase error between $\pm 0.25T_{VCO}$ where T_{VCO} is the VCO period. Outside this range, the phase detection gain becomes negative, which makes the negative feedback loop become a positive feedback loop and the PLL unstable. Because its phase detection gain depends on the oscillation amplitude, A_{VCO}, which is limited by the supply voltage, the sub-sampling detection gain is limited, which in turns increases the charge pump noise contribution. To boost the detection gain and extend the detection range, the clock-skew-sub-sampling technique is proposed as shown in Fig. 2.3.3. Instead of directly sampling the VCDL output, a re-timer is added to re-time the frequency divider output DIV from the first stage by the rising edge of the VCDL output, and the output of the re-timer $VCDL_{RE}$ is then sampled. As such, the positive detection range is extended from $\pm 0.25T_{VCO}$ to $\pm 0.5T_{ref}$, where T_{ref} is the reference period. For the same rising slopes, k, of VCDL and $VCDL_{RE}$, the clock-skew sub-sampling and the sub-sampling have the same gain $T_{VCO}\cdot k/2\pi$. With the clock-skew sub-sampling, a higher phase-detection gain is achieved by reducing the rise time to increase rising slope k instead of using a higher supply voltage. To further enhance the phase-detection gain, a time amplifier [5] is used to amplify the input phase error before being detected by the clock-skew sub-sampling PD, which effectively reduces the rise time and increases the rising slope k. With a 120ps rise time and a time-amplifier gain of 5 at a 1.2V supply, the phase-detection gain of the proposed time-amplified clock-skew-sub-sampling PD becomes equivalent to sub-sampling with a VCO amplitude of 4V at 2.1GHz.

The proposed cascaded PLL is fabricated in a 65nm CMOS process, occupies $0.043mm^2$ area, and consumes 3.84mW. Figure 2.3.4 shows the measured output phase noise spectra of the Type-II PLL and the cascaded PLL with the reference frequency of 67.74MHz and bandwidths of 10MHz and 40MHz. With the 10MHz-bandwidth configuration for minimum jitter, the cascaded PLL measures phase noise at 1MHz offset of -108.3dBc/Hz and integrated jitter (from 1KHz to 50MHz) of 1.05ps (as compared to -93.3dBc/Hz and 3.67ps at the output of the first stage, respectively). With the 40MHz-bandwidth configuration for minimum in-band phase noise, the in-band phase noise at 100KHz offset is suppressed by 24dB from -88.6dBc/Hz at the first-stage output to -112.6dBc/Hz at the output of the cascaded PLL. From the phase noise spectrum, the -3dB bandwidth can reach 40MHz even with the reference frequency as low as 67.74MHz. With a VSA89600 vector signal analyzer, the Type-II PLL and the cascaded PLL measure settling time of 4.0μs and 4.2μs, respectively, showing that the clock-skew sub-sampling DLL has an insignificant degradation of the settling time. To test the supply rejection, a -74dBm 1MHz noise source is applied to the RO supply, and, as shown in Fig. 2.3.5, the 1MHz spurs are measured to be -22dBc at the first-stage output and -46dBc at the cascaded PLL output. Figure 2.3.6 summarizes and compares the performance with existing integer-N PLLs. Figure 2.3.7 shows the die micrograph.

Acknowledgment:
This project was supported in part by the Hong Kong General Research Funding (16206614) and the National Nature Science Foundation of China (61306030)

References:

[1] A. Sai et al., "A Digitally Stabilized Type-III PLL Using Ring VCO with $1.01ps_{rms}$ Integrated Jitter in 65nm CMOS," *ISSCC Dig. Tech. Papers*, pp. 248-249, Feb. 2012.
[2] J. Lee and H. Wang, "Study of Sub-harmonically Injection-Locked PLLs," *IEEE J. Solid-State Circuits*, vol. 44, no. 5, pp. 1539-1553, May. 2009.
[3] L. Kong and B. Razavi, "A 2.4GHz 4mW Inductor-less RF Synthesizer," *ISSCC Dig. Tech. Papers*, pp. 450-451, Feb. 2015.
[4] X. Gao et al., "Spur-Reduction Techniques for PLLs Using Sub-Sampling Phase Detection," *ISSCC Dig. Tech. Papers*, Feb. 2010.
[5] S.-K. Lee et al., "A 1GHz ADPLL with a 1.25ps Minimum Resolution Sub-Exponent TDC in 0.18um CMOS," *ISSCC Dig. Tech. Papers*, Feb. 2010.

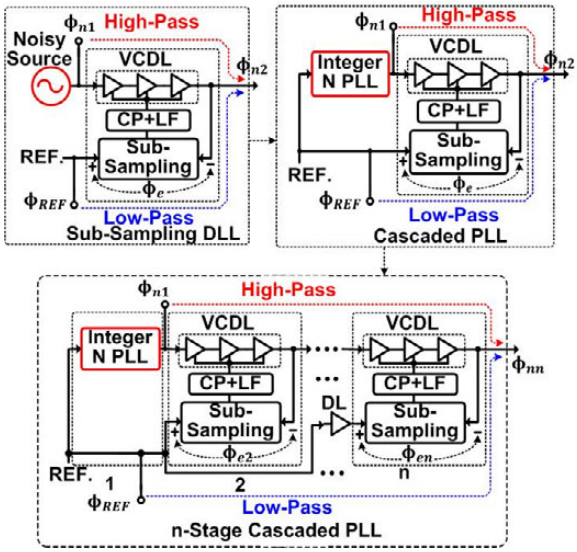


Figure 2.3.1: Illustration of the proposed cascaded PLL concept.

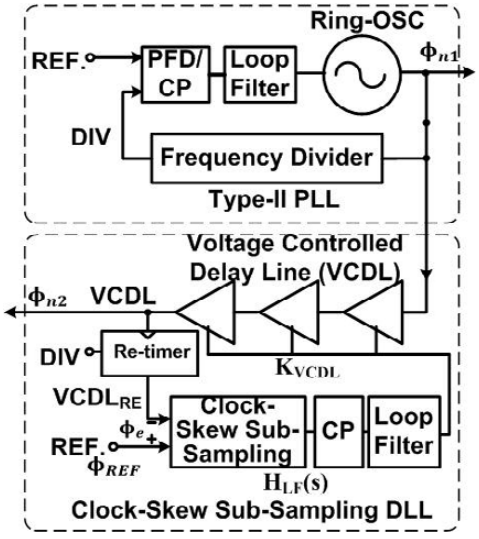


Figure 2.3.2: Block diagram of the proposed PLL with a cascaded clock-skew sub-sampling DLL.

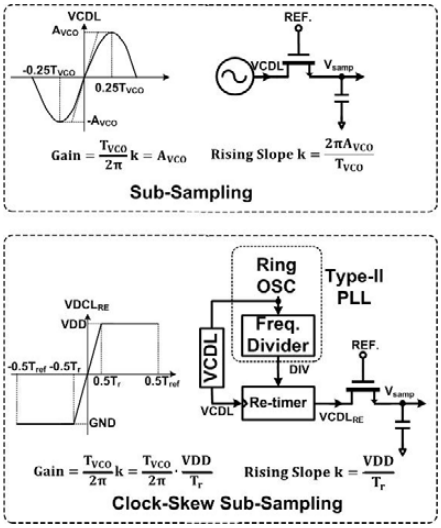


Figure 2.3.3: Comparison of the conventional sub-sampling and the proposed clock-skew sub-sampling techniques.

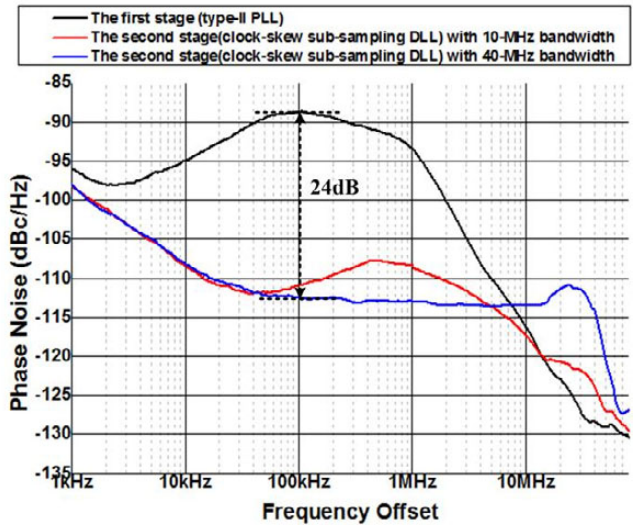


Figure 2.3.4: Measured output phase noise of the Type-II PLL and of the cascaded PLL with 10MHz and 40MHz bandwidths.

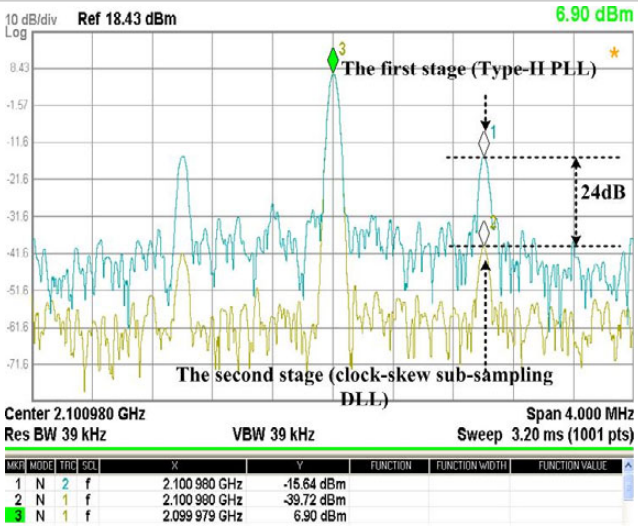


Figure 2.3.5: Measured output spectra of the Type-II PLL output and of the cascaded PLL with -74dBm 1MHz VCO supply noise injected.

	[1]	W. Deng, ISSCC'14	[3]	Y. C. Huang, ISSCC'14	[4]	This Work
PLL Architecture	Type-III PLL	IL-PLL	Type-I PLL	ADPLL	Sub-sampling	Cascaded PLL
VCO Type	Ring	Ring	Ring	Ring	LC	Ring
Output Freq.	3.24 GHz	0.9 GHz	2.39 GHz	2.418 GHz	2.21 GHz	2.1 GHz
Freq. Tuning Range	1.4-3.2 GHz	0.39-1.41 GHz	2.0-3.0 GHz	N/A	N/A	1.1-2.1 GHz
Ref. [MHz]	108	150	22.6	26	55.25	67.74
Multi. Ratio	30	6	106	93	40	31
In-band PN [dBc/Hz]	-110	N/A	-114	-94	-121	-113
Integrated Jitter	1.01ps	1.7ps	0.97ps	3.3ps	0.3ps	1.05ps
Power [mW]	27.5	0.78	4	6.4	3.8	3.84
FOM* [dB]	-225.5	-236.5	-234.2	-223.5	-245	-234
Settling Time	85 us	N/A	N/A	N/A	N/A	4.2 us
Ref. Spur	N/A	-41dBc	-65dBc	-75dBc	-80dBc	-45dBc
VDD [V]	1.2	0.8	1	1.1	1.2	1.2
Core Area [mm²]	0.32	0.0066	0.015**	0.013	0.2	0.043
Process	65nm CMOS	65nm CMOS	65nm CMOS	40nm CMOS	180nm CMOS	65nm CMOS

*FOM = 20 log(Integrated Jitter) + 10log(Power/1mW)

** Active Area

Figure 2.3.6: Measured performance summary and comparison with existing integer-N PLLs.

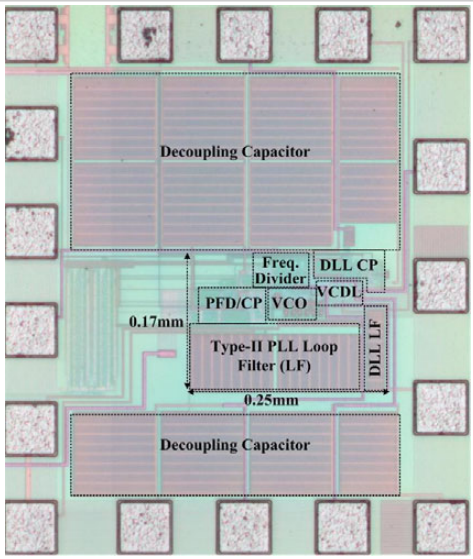


Figure 2.3.7: Die micrograph.

978-1-4673-9467-3/16/$31.00 ©2016 IEEE

2.4 A 2-to-16GHz BiCMOS ΔΣ Fractional-N PLL Synthesizer with Integrated VCOs and Frequency Doubler for Wireless Backhaul Applications

Tino Copani, Claudio Asero, Matteo Colombo, Paolo Aliberti, Giuseppe Martino, Francesco Clerici

STMicroelectronics, Catania, Italy

The flourishing of ubiquitous wireless communication networks has pushed the development and deployment of complex RF telecom systems. Concurrently, the IC industry has been making an effort to increase the integration of RF devices. While nanometer CMOS technologies are now dominating end-user devices, the RF domain of wireless infrastructure still suffers from low-scale of integration [1]. Nonetheless, wireless backhaul vendors are now upgrading existing systems, which rely on expensive discrete technologies (i.e. GaAs), and adopting BiCMOS RFICs. A local oscillator (LO) synthesizer is a key block in the implementation of any wireless transceivers. Very tight requirements, in terms of frequency stability and phase noise performance, have led to complex PLL-based monolithic synthesizers. For instance, multi-bit capacitor array VCOs allow the reduction of the VCO tuning gain (*Kvco*), improving phase-noise performance without frequency coverage penalties. A ΔΣ fractional-*N* approach has been also introduced to optimize frequency resolution, lock time and noise performance of PLL-based synthesizers [2].

A 2-to-16GHz SiGe BiCMOS LO synthesizer for wireless backhaul is presented in this work. Figure 2.4.1 shows the architecture of the PLL-based synthesizer. The IC consists of a 21b-MASH 1-1-1 ΔΣ fractional-*N* PLL with integrated VCOs and LDO regulators. A bank of 4 VCOs with 5b programmable LC-tanks allows the frequency coverage from 4 to 8GHz regardless of process variations, device aging and -40 to 85°C thermal excursions. A monolithic frequency doubler and a high-speed prescaler extend the LO frequency range. Two 100Ω internally-matched differential buffers are used at the IC output. A 4.5V low-noise high-current LDO regulator supplies the VCOs and the PLL charge pump, while 2.5V regulators are used elsewhere. The PLL system features fast locking through a reconfigurable loop-filter response and a cycle-slip prevention mechanism. The simplified schematic of one LC-VCO is reported in Fig. 2.4.2.

An automatic PLL calibration selects VCOs and LC-tank switches upon device frequency programming through a serial interface (SPI), while an amplitude-control scheme sets the VCO output swing through Vb. Low-voltage MOS switches are used in the 5b capacitor array, whereas bipolar varactors (D_v) are used for VCO locking. Wireless infrastructure applications require that, once programmed, the LO synthesizer maintained frequency lock when temperature spans the entire range (thermal cycling). Generally, the VCO phase noise improves when the signal amplitude at the LC-tank nodes is maximized [3]. However, varactors forward bias limits the achievable signal amplitude when tuning voltage (V_{tune}) approaches a low value during a thermal cycle. To improve the VCO performance, a negative supply block can be enabled to provide varactors with a -0.7V bias (V_{neg}) through L_b chokes. The negative supply block is implemented with a switched-capacitor approach. Switching clock phases (ϕ_P, ϕ_N) are derived from the PLL prescaler to minimize spur tones. Moreover, to avoid out-of-band tones and allow for better filtering through C_{neg} and L_b, the switching clock runs just at half the VCO frequency. High-speed, low-voltage MOS switches are used to optimize the negative supply efficiency. Nevertheless, the achievable negative supply voltage is limited at multi-GHz clock frequencies. Therefore, V_{neg} is clamped to -0.7V to keep the negative supply constant over the VCO frequency range. Circuit simulations proved that adopted V_{neg} can guarantee reverse bias of the VCO varactors at the maximum signal amplitude over thermal cycles.

Monolithic frequency doublers are usually implemented exploiting mixing architectures [4] or rectification through active device pairs. Mixer-based topologies offer wideband operation and good I/O reverse isolation but are power hungry and noisy. Rectification-based doublers offer low noise and power savvy characteristics but show poor I/O isolation and harmonic rejection. Figure 2.4.3 shows the proposed autotransformer-based frequency doubler, which alleviates these issues and improves the conversion gain of rectifier-based doublers. A differential bipolar pair (Q_1, Q_2) with tied collectors and emitters is used to exploit 2nd-order harmonic generation through junction rectification. Load resistors (R_c, R_e) with peaking inductors (L_c, L_e) allow the broadband operation. Peaking inductors are implemented as vertically stacked coils to exploit mutual coupling. This technique increases the doubler gain and guarantees 180° phase shift between the differential outputs, improving supply noise rejection and decreasing leakage back to the doubler input. Furthermore, the frequency doubler with the coupled inductors allows the achievement of better phase-noise performance than that of prior common realizations. The frequency doubler block drives a 100Ω internally-matched output buffer as shown in Fig. 2.4.3. The output buffer is based on a Cherry-Hooper design, modified to offer broadband operation and output matching. IC double wirebonds are exploited as peaking inductors to tune out stray capacitances of active devices and bondpads.

High-speed prescalers have become critical blocks in many RF applications. Current-mode logic (CML) D-latch prescalers achieve very high-speed operation with moderate power dissipation [1]. However, low supply voltage of latest technologies makes the design of static CML prescalers a challenging task. Alternatively, injection-locked prescalers can be effectively used but they show a narrow frequency range and require bulky resonators. The schematic of a Class-AB divide-by-two prescaler is shown in Fig. 2.4.4. Triple-tail CML gates are used in the D-latches for low-supply voltage operation. Coupling capacitors C_c speed-up read-to-latch transitions by dynamically increasing and decreasing the current supplied to the triple-tail gates. Small HBTs (Q_3, Q_4 and Q_5, Q_6) avoid loading prescaler driving stages but show high base resistance (r_b), which reduces HBT f_{max} and the latch speed. Emitter degeneration capacitors (C_e) are used to reduce the impact of r_b on prescaler performance. However, C_e degeneration capacitors set a lower bound to prescaler frequency range. Nonetheless, inherent low quality factor of R_eC_e relaxation tank (i.e., Q=1) [3] guarantees a much larger frequency range than that of injection-locked dividers with high-Q LC resonators.

The BiCMOS synthesizer IC is packaged in a 36-pin QFN carrier. Internal programmable LDO regulators require a 2.7V supply for PLL blocks and 5V for the VCOs. High-voltage supply can be set to 3.3V if the application does not require best VCO performance. Figure 2.4.5 shows measured LO phase noise at different frequencies for a 60kHz PLL bandwidth and 50MHz reference frequency. Phase noise is -135dBc/Hz at 1MHz offset from a 4GHz carrier, while it is -122dBc/Hz for a 16GHz output frequency. Figure 2.4.6 shows the IC output power against the LO frequency. The output power is as high as +5dBm at 13GHz. The VCO fundamental leakage at the frequency doubler output is also shown in Fig. 2.5.6. The VCO rejection is higher than 20dB across the doubler frequency range. The IC die size is 2.9x3.0mm² including pads and its power consumption is 1116mW. Die micrograph is reported in Fig. 2.5.7.

References:

[1] S. Yu et al., "A Single-Chip 125-MHz to 32-GHz Signal Source in 0.18-µm SiGe BiCMOS," *IEEE J. Solid-State Circuits*, vol. 46, no. 3, pp. 598-614, Mar. 2011.

[2] M. Kennedy et al., "0.3–4.3 GHz Frequency-Accurate Fractional-*N* Frequency Synthesizer with Integrated VCO and Nested Mixed-Radix Digital Δ–Σ Modulator-Based Divider Controller," *IEEE J. Solid-State Circuits*, vol. 49, no. 7, pp. 1595-1605, July 2014.

[3] B. Razavi, "A Study of Phase Noise in CMOS Oscillators," *IEEE J. Solid-State Circuits*, vol. 31, no. 3, pp. 331-343, Mar. 1996.

[4] L. Vera et al., "An Active Frequency Doubler with DC-100 GHz Range," *IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, pp. 9–12, Oct. 2014.

 978-1-4673-9467-3/16/$31.00 ©2016 IEEE

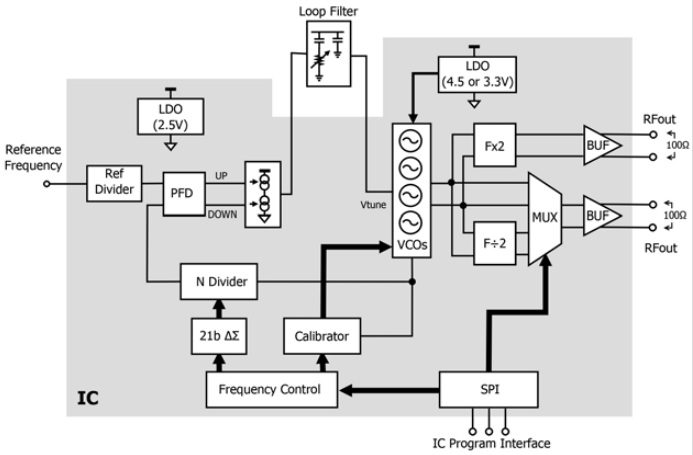


Figure 2.4.1: Architecture of the LO synthesizer. Blocks in the shaded area are implemented on-chip.

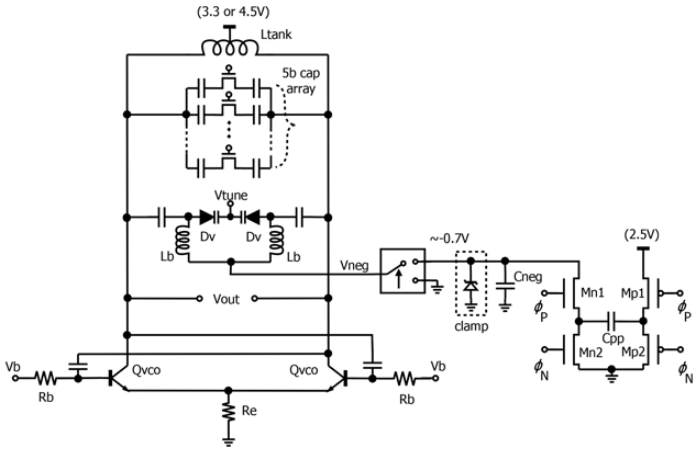


Figure 2.4.2: Schematic of the adopted VCO design with a negative supply source.

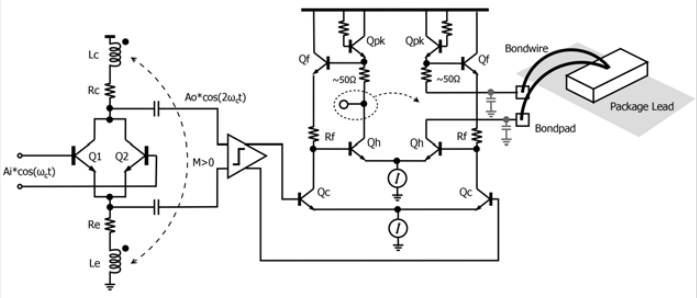


Figure 2.4.3: Simplified schematic of a frequency doubler and a broadband output buffer.

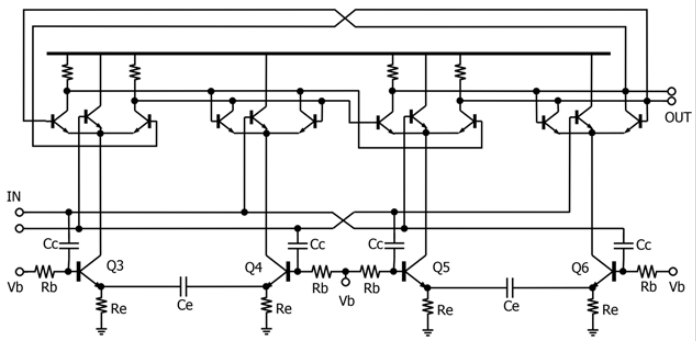


Figure 2.4.4: Simplified schematic of the Class-AB divide-by-two stage.

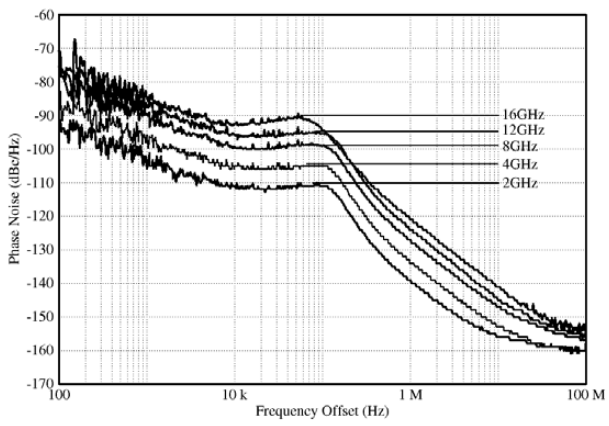


Figure 2.4.5: LO phase noise measurement results at different output frequencies.

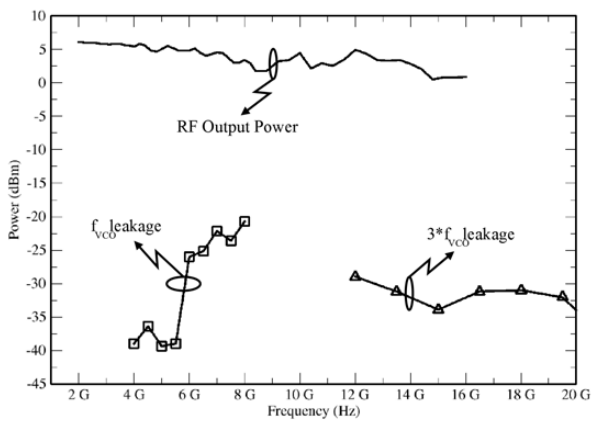


Figure 2.4.6: LO synthesizer output power and harmonic leakage at the doubler output.

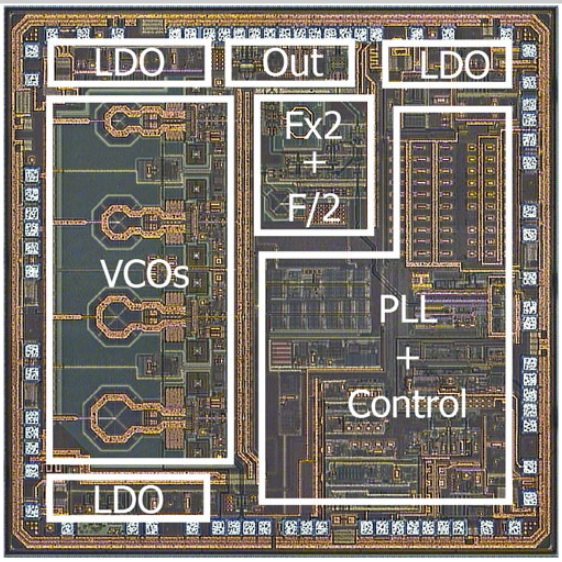


Figure 2.4.7: Die micrograph.

978-1-4673-9467-3/16/$31.00 ©2016 IEEE

2.5 A Complementary VCO for IoE that Achieves a 195dBc/Hz FOM and Flicker Noise Corner of 200kHz

David Murphy, Hooman Darabi

Broadcom, Irvine, CA

An LC oscillator can achieve near optimal performance if the common-mode of the circuit is designed to resonate at twice the oscillation frequency [1-3]. Common-mode resonance can be accomplished with an *explicit* tail inductor [1] or *implicitly* by designing the primary resonant tank such that the differential mode is half the common-mode [2,3]. Figures 2.5.1a and 2.5.1b show the NMOS-only and complementary versions [4] of Hegazi's explicit common mode resonance topology, while Fig. 2.5.1c shows a design that employs implicit common-mode resonance. Implicit common-mode resonance has the advantage of a more easily controlled and modelled common-mode and requires one less inductor, but so far has only been applied to NMOS-only oscillators [2,3]. The primary advantage of an NMOS-only design is that, for a given inductance, lower absolute phase noise can be achieved owing to the larger maximum output swing; however, a complementary design is more suitable for low-power applications with more modest phase-noise specifications (such as IoE) where phase noise per unit current and area is important. With an eye to such applications, this paper extends the concept of implicit common-mode resonance to an ultralow power complementary design (i.e. the missing topology in Fig. 2.5.1d).

To arrive at the complementary design, we begin with separate NMOS and PMOS designs biased across $V_{DD}/2$ as shown in Fig. 2.5.2. Both the NMOS and PMOS circuits oscillate at the same frequency and are designed such that their respective tanks have a common-mode resonance frequency that is twice the oscillation frequency. Because the oscillators share the same silicon, some non-zero magnetic coupling between the two inductors exists and the oscillators frequency-lock together, which reduces phase noise by 3dB (compared to a single oscillator biased from $V_{DD}/2$). Current reuse can then be employed if the center tap of both inductors are shared. Moreover, the two inductors can be merged into a single strongly coupled transformer with a resulting 50% area saving. Shorting the center tap of the resultant tightly coupled transformer ensures that only one differential mode and only one common mode can ever be excited, thereby ensuring that the essentially coupled oscillators lock with the phase arrangement shown in Fig. 2.5.3.

As shown in [2,5], an oscillator figure-of-merit (FOM) can be written in terms of oscillator power efficiency, η, and Leeson's noise factor, F, as

$$\text{FOM}=\frac{\left(\frac{\omega}{\Delta\omega}\right)^2}{\text{L}\{\Delta\omega\}\text{P}_{\text{DC[mW]}}}=\frac{2\eta\text{Q}^2}{\text{kTF}}10^{-3}.$$

Furthermore, it is noted that the maximum possible value of η/F is 1/(1 + γ), where γ (≈0.67) is the channel-noise coefficient of a CMOS device. This means, that in dB, the best possible performance of any CMOS LC oscillator is $\text{FOM}_{\text{MAX}} = 174.6+20\log_{10}\text{Q}$. Just like its NMOS-only counterpart [2] and Hegazi's original design, the complementary topology presented in this work approaches this fundamental limit. Figure 2.5.3 shows an idealized version of the proposed topology where the ratio of single-ended to differential capacitance is set by means of the variable X. If the common-mode is correctly tuned, such as in this example when the variable X is set to 0.65, the FOM is maximized and gets to within 1dB of the theoretical optimum for the given tank Q. In other words, Leeson's noise factor, F, approaches 1 + γ, and oscillator power efficiency, η, reaches 80%. Just like the NMOS-only design, flicker noise is also completely nullified in the complementary design owing to the perfect phase alignment of the 1st and 2nd harmonics (see presentation slides associated with [2]).

As well as matching the theoretical performance of the NMOS-only design, the proposed complementary design has a number of practical advantages. As the maximum swing in the core is only around V_{DD}, minimum length thin-oxide devices can be used throughout the circuit (unlike the NMOS-only design where the output swing exceeds $2V_{DD}$ and so requires thick oxide I/O devices to avoid breakdown issues). Thin-oxide devices in the switched capacitor bank result in higher Qs for the same on/off range (nearly 2× higher compared to thick-oxide devices in 28nm), while thin-oxide devices in the differential pair correspond to a larger negative resistance per unit capacitance (in 28nm, a thin-oxide complementary negative resistance has ~40% less capacitance than an equivalent NMOS-only thick-oxide negative resistance). Both these features allow for improved performance at higher frequencies.

A 28nm prototype of the proposed design was fabricated for use in a low-power transceiver operating in the 2.4GHz ISM band, which is suitable for IoE applications. To simplify I/Q generation such a receiver typically requires a 4.8GHz VCO. The designed transformer had an effective differential inductance of 3.7nH at 5GHz while the common-mode inductance was 1.55nH at 10GHz. The spacing between the transformer windings was purposefully increased to boost the common-mode Q, which resulted in a coupling coefficient of k = 0.4. As in the original NMOS-only design, the ratio of differential to single-ended capacitance is given by

$$\frac{\text{C}_{\text{DM}}}{\text{C}_{\text{CM}}}=\frac{3\text{-}5\text{k}}{1+\text{k}}.$$

The measured tuning range of the fabricated VCO was 4.7 to 5.4GHz and 0.7mA was drawn from a 0.7V supply. Figure 2.5.4 shows the measured phase-noise profile and FOM profile versus carrier offset for four different frequency settings. Note that the FOM (in the thermal noise region) is always better than 194dBc/Hz, and the flicker noise corner is around 200kHz. Figure 2.5.5 shows the phase noise, FOM and flicker noise corner (measured as the frequency at which the FOM degrades by 3dB from the FOM at 5MHz) versus oscillation frequency. The peak FOM is 196dBc/Hz@10MHz at 4.85GHz, and the high FOM and the low flicker noise corner are maintained across the band. Because the VCO is voltage biased, by monitoring the current and assuming an efficiency of around 65%, we can calculate the effective *Q* of the tank as approximately 13. Figure 2.5.6 compares our work to current state-of-the-art VCOs. The FOM matches the performance of Hegazi's gold-standard NMOS-only VCO [1] but requires no additional inductor. In addition, it has a similar tuning range and operates from a much lower supply voltage (0.7V versus 2.5V) and a higher frequency (5GHz versus 1.8GHz).

Compared to best reported CMOS topology [4] in Fig 2.5.6, we achieve a similar FOM at 10MHz and a comparable tuning range, but we measure a notably lower flicker noise corner such that FOM measured at a 100kHz offset is 3 to 6dB better (as a reference, a 3dB improvement in FOM corresponds to 2× saving in power). As the flicker noise corner is sensitive to accurate common-mode resonance (see Fig. 2.5.3), this suggests the *implicit* common-mode resonance technique may have a practical advantage over the *explicit* common-mode resonance technique used in [4].

References:

[1] E. Hegazi et al., "A filtering technique to lower LC oscillator phase noise," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 1921-1930, Dec. 2001.

[2] D. Murphy et al., "A VCO with implicit common-mode resonance," *ISSCC Dig. Tech. Papers*, pp. 346-347, 442-443, Feb. 2015.

[3] M. Shahmohammadi et al., "A 1/f noise upconversion reduction technique applied to Class-D and Class-F oscillators," *ISSCC Dig. Tech. Papers*, pp. 444-445, Feb. 2015.

[4] M. Garampazzi et al., "Analysis and Design of a 195.6 dBc/Hz Peak FoM P-N Class-B Oscillator With Transformer-Based Tail Filtering," *IEEE J. Solid-State Circuits*, vol. 50, no. 7, pp. 1657–1668, July 2015.

[5] D. Murphy et al., "Advances in the design of wideband receivers," *IEEE Custom Integrated Circuits Conference*, pp. 1-8, Sept. 2013.

 978-1-4673-9467-3/16/$31.00 ©2016 IEEE

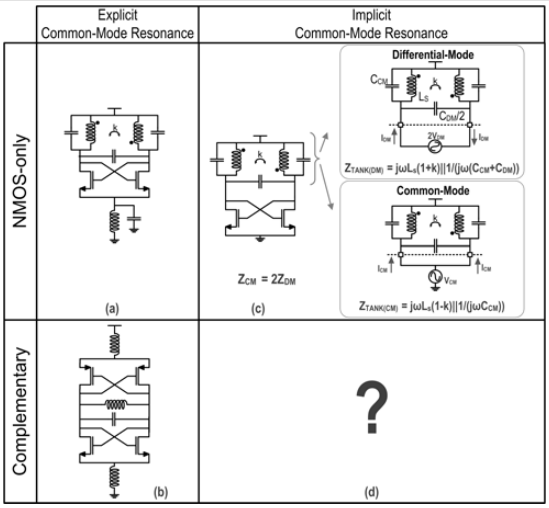


Figure 2.5.1: Known VCO topologies that employ explicit or implicit common-mode resonance. No complementary topology that employs implicit common-mode resonance has yet been reported.

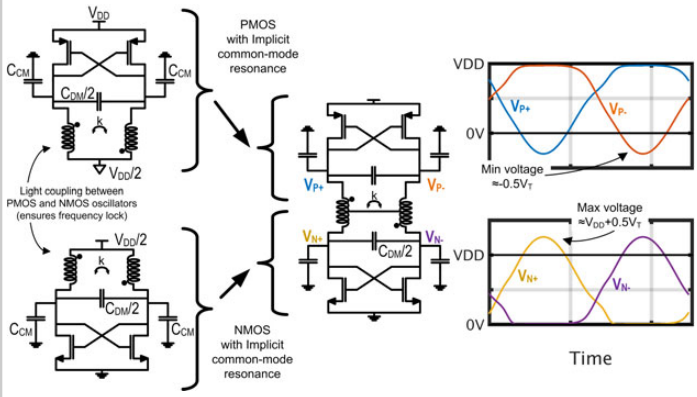


Figure 2.5.2: Proposed complementary oscillator with implicit common-mode resonance is constructed by merging a PMOS-only and an NMOS-only design. Because of current reuse, a single transformer can be used. The CMOS structure ensures the oscillation waveform does not significantly exceed VDD.

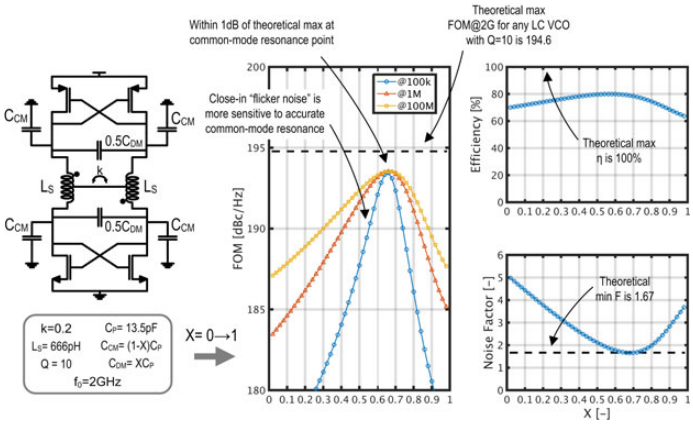


Figure 2.5.3: By varying the ratio of single-ended to differential capacitance, common-mode resonance can be achieved. At this point efficiency reaches 80%, Leeson's noise factor drops to 1.67 and the FOM gets within 1dB of the theoretical maximum.

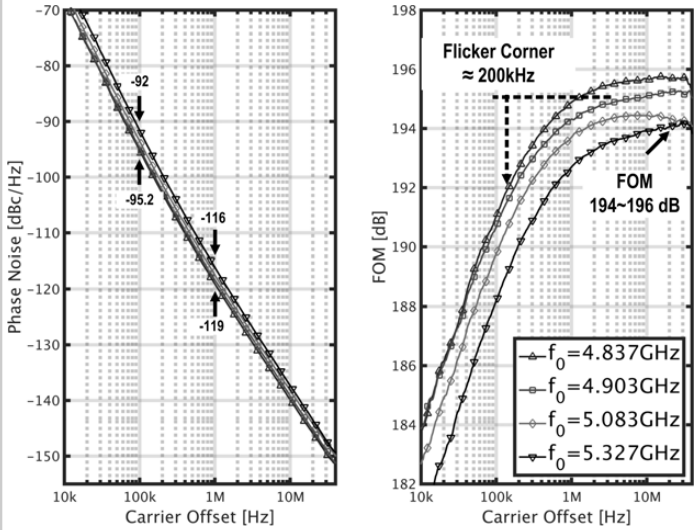


Figure 2.5.4: Measured phase noise and figure of merit versus carrier offset.

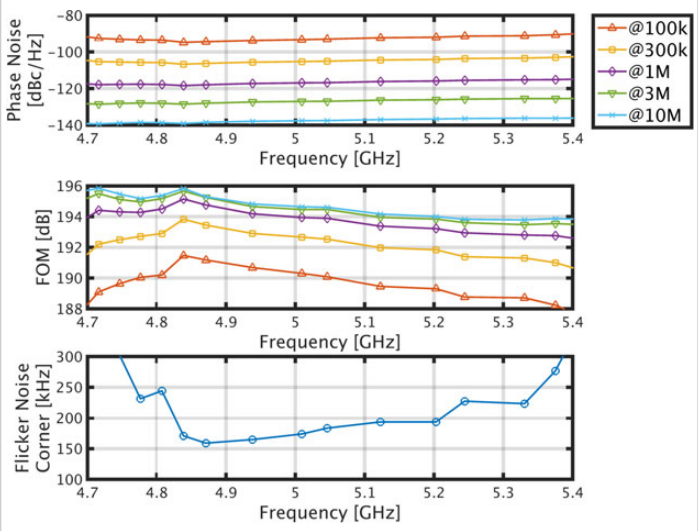


Figure 2.5.5: Performance metrics versus oscillation frequency.

	JSSC 2001 [1]	ISSCC 2015 [7]	JSSC 2015 [4]	This Work
Topology	NMOS-only $2F_{LO}$ Explicit Resonance	NMOS-only $2F_{LO}$ Implicit Resonance	Complementary $2F_{LO}$ Explicit Resonance	Complementary $2F_{LO}$ Implicit Resonance
Technology	0.35 µm	28 nm	55nm	28nm
Supply Voltage	2.5	0.9	1.5	0.70
Tuning Range	1-1.2 (18%)	2.85-3.75 (27.2%)	7.4-8.4 (13%)	4.7-5.4 (13.8%)
Phase Noise [dBc/Hz @ 3 MHz]	-153.2	-139.6	-133	-126.9
Power [mW]	9.1	6.8	6.3	0.5
FOM [dB] (Thermal noise region)	194.5	192.2	194.3-195.6	**194-196**
FOM [dB] @100kHz	≈185*	186.5-188.1	≈185*	**188-191**
Core Area [mm²]	N/A	0.19	0.19	0.18
Inductors	2	1	3	1 XFMR

*Estimated from plots

Figure 2.5.6: Comparison table.

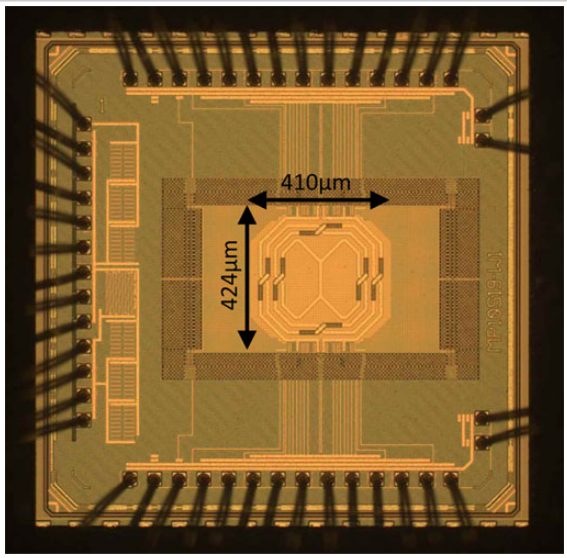


Figure 2.5.7: Die micrograph.

978-1-4673-9467-3/16/$31.00 ©2016 IEEE

2.6 A 190.5GHz Mode-Switching VCO with 20.7% Continuous Tuning Range and Maximum Power of -2.1dBm in 0.13μm BiCMOS

Rouzbeh Kananizadeh, Omeed Momeni

University of California, Davis, CA

Wideband mm-Wave and terahertz (THz) applications, including high data-rate communications, high-resolution radar and spectroscopy, require wideband signal sources. Nevertheless, low quality factor of varactors and lossy switches in addition to relatively large parasitic capacitors of transistors have been limiting the tuning range of voltage controlled oscillators (VCO) at these frequencies. To overcome these challenges, harmonic VCOs using high harmonic numbers and switched-capacitor banks at much lower fundamental frequencies were reported [1]. The drawback to this approach is the limited output power since the extracted harmonic number is typically high. Other tuning techniques such as phase/delay control between coupled oscillators and tuning boosting using transformer-based resonators were also reported [2-4]. However, the highest reported tuning range for VCOs above 150GHz is not more than 12.5%, which covers a small portion of the bandwidth available at high mm-Wave and THz frequencies.

Mode switching VCOs at frequencies below 10GHz have shown outstanding tuning ranges. However, existing low-frequency techniques are challenging to exploit at sub-THz frequencies since high parasitic capacitors of mode switching devices result in very narrow tuning ranges. Moreover, losses in mode-switching devices can impede oscillation start-up and thus dramatically reduces its harmonic power generation. To tackle these issues, a system of coupled oscillators using an active mode-switching (AMS) block is presented. The proposed VCO is implemented in a 0.13μm BiCMOS technology, confirming 20.7% of tuning range at center frequency of 190.5GHz with the maximum output power of -2.1dBm.

Figure 2.6.1 shows the circuit diagram of the system. The two main oscillators, OSC_West (OSC_W) and OSC_East (OSC_E) have a differential Colpitts structure in which the oscillator tanks are located at the bases of the HBTs and identified by b.SW, b.SE, b.NW and b.NE. The AMS blocks are connected directly to the tanks of the Colpitts oscillators. By turning the AMS blocks off or on, the two oscillators operate in-phase (even mode) or out-of-phase (odd mode), respectively. In the even mode, the proposed AMS block loads each tank with low-loss and low-capacitance admittance; therefore, they do not deteriorate harmonic power generation and tuning range. In the odd mode, AMS has loss-cancelling and capacitance-tuning behavior. As a result, significant improvement in the second harmonic output power and tuning range is achieved. The two modes have distinct center frequencies. They cover different frequency bands with an overlap, which result in a wide overall tuning range. The layout of the circuit has the same symmetry and placement as the block diagram in Fig. 2.6.1. Circuit nodes, located on the dashed horizontal line crossing the two oscillators, are always at virtual ground (V.G.).

Even mode is the higher frequency mode and is invoked when the AMS blocks are turned off by setting V_{on2} to 0V. In this mode, the two oscillators, OSC_W and OSC_E, are in-phase as shown in Fig. 2.6.2. The oscillators, OSC_W and OSC_E, share lines, T1, at the emitters of Q1/Q3, and Q2/Q4. In the even mode, T1 results in a higher impedance at the emitters, and consequently the negative conductance at the tanks is increased for a stronger oscillation. Moreover, in-phase mode of oscillation results in lower loss from the AMS blocks as shown in Fig. 2.6.2. The equivalent circuit of the AMS block in the even mode is also shown in Fig. 2.6.2. Here, all the nodes on the vertical dashed line crossing the AMS blocks are common-mode nodes. As a result, 4kΩ resistors are in series with the varactors in the equivalent circuit, and thus the lossy and capacitive effects of the varactors on the tanks are reduced. The bias voltage of the emitters in the AMS blocks is set to 1V through 2kΩ resistors while the bias voltage at the bases of the transistors is 1.5V. This leaves a small junction capacitor at the base-emitter junction of the transistors Q5, Q6, Q7 and Q8 in the AMS blocks. Furthermore, the inductance from the line, T3, at the emitter resonates with the parasitic capacitors at this node. These design techniques cause the input admittance of the AMS blocks to have low-loss and low-capacitance loading effects on the tanks over a wide frequency range. This enables the VCO to reach higher operation frequencies.

Odd mode is selected when the AMS blocks are turned on by setting V_{on2} to 1.5V. The AMS blocks present a high negative conductance to the tanks of the oscillators if the transistor bases (e.g. b.SW and b.SE) are out-of-phase. This forces the oscillators to switch to the odd mode of operation. The equivalent circuit in this mode is shown in Fig. 2.6.3. All nodes on the vertical dashed line crossing the AMS blocks are virtual ground. Thus, unlike the even mode, the varactors can change capacitance at the tanks and contribute to tuning. They can also control the frequency overlap between the two modes of operation. In the odd mode, the relatively long line, T2, does not load the collectors of each of the AMS blocks, which results in a stronger oscillation. As shown in Fig. 2.6.3, the input capacitance at the bases of transistors Q5, Q6, Q7 and Q8 increases compared to the even mode in Fig. 2.6.2 and thus, the oscillation frequency drops.

Transmission lines at the collector of the HBTs in the main oscillators are designed to achieve the optimum condition for strong oscillation [5]. The second harmonic power was extracted from OSC_E. The microstrip transmission lines are implemented using the top metal layers. Metal-Oxide-Metal capacitors, all lines and their interactions are fully simulated using a three-dimensional electromagnetic simulator. Simulated performance of the MOS-based varactors is illustrated in Fig. 2.6.4. For C_{max} over C_{min} ratio of 2.4 at 100GHz, quality factor of the varactors varies between 2.7 and 10.2. These quality factors are nearly half of the ones in a typical 65nm CMOS process and have direct impact on output power and phase noise performance of the VCO.

Figure 2.6.5 illustrates the measurement setup. Measurement results, including tuning range, output power and phase noise, are reported in Fig. 2.6.4. These results confirm frequency tuning from 170.8GHz to 195.6GHz (13.6% tuning range) in the odd mode and 193.5GHz to 210.1GHz (8.3% tuning range) in the even mode. As a result, an excellent tuning range of 20.7% at the center frequency of 190.5 GHz is measured. This is significantly wider than the prior art reported in Fig. 2.6.6 for G-band frequencies and above. The maximum output power is -2.1dBm at 194.8GHz in the odd mode. This VCO dissipates a maximum DC power of 294mW in the odd mode and 183mW in the even mode from a 2.1V supply. Fig. 2.6.6 compares the performance of the implemented VCO with prior art. Fig. 2.6.7 shows the die micrograph. The symmetric layout assists with a more robust performance of the VCO. The VCO occupies 0.25mm^2 excluding the pads.

Acknowledgements:
The authors would like to thank the National Science Foundation for supporting this project. They also like to thank Hossein Jalili and all lab members for their assistance.

References:
[1] J. Zhang et al., "85-to-127 GHz CMOS Signal Generation Using a Quadrature VCO with Passive Coupling and Broadband Harmonic Combining for Rotational Spectroscopy," *IEEE J. Solid-State Circuits*, vol. 50, no. 6, pp. 1361-1371, June 2015.
[2] M. Adnan and E. Afshari, "A 247-to-263.5GHz VCO with 2.6mW Peak Output Power and 1.14% DC-to-RF Efficiency in 65nm Bulk CMOS," *ISSCC Dig. Tech papers*, pp.262-263, Feb. 2014.
[3] Y. Tousi et al., "A 283-to-296GHz VCO with 0.76mW Peak Output Power in 65nm CMOS," *ISSCC Dig. Tech. Papers*, pp. 258-260, Feb. 2012.
[4] H. Koo et al., "Design and Analysis of 239 GHz CMOS Push-Push Transformer-Based VCO with High Efficiency and Wide Tuning Range," *IEEE Trans. Circuits and Systems-I*, vol. 62, no. 7, pp. 1883-1893, July 2015.
[5] O. Momeni and E. Afshari, "High Power Terahertz and Sub-Millimeter-Wave Oscillator Design: A Systematic Approach," *IEEE J. Solid-State Circuits*, vol. 46, no. 3, pp. 583-597, Mar. 2011.
[6] R. Han, E. Afshari, "A 260GHz Broadband Source with 1.1mW Continuous Wave Radiated Power and EIRP of 15.7dBm in 65nm CMOS," *ISSCC Dig. Tech. Papers*, pp. 138-139, Feb. 2013.
[7] P.-Y. Chiang et al., "A Silicon-Based 0.3 THz Frequency Synthesizer with Wide Locking Range," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 2951-2963, Dec. 2014.

 978-1-4673-9467-3/16/$31.00 ©2016 IEEE

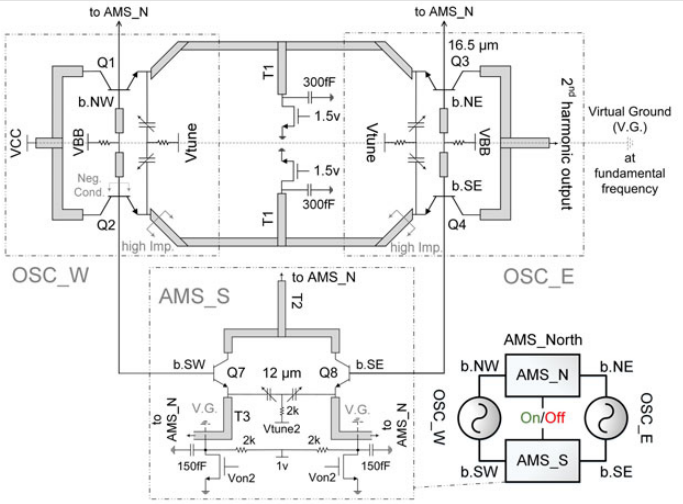


Figure 2.6.1: Block-level and circuit-level diagram of the proposed VCO including the main oscillators (OSC_E and OSC_W) and the active mode-switching blocks (AMS_S and AMS_N).

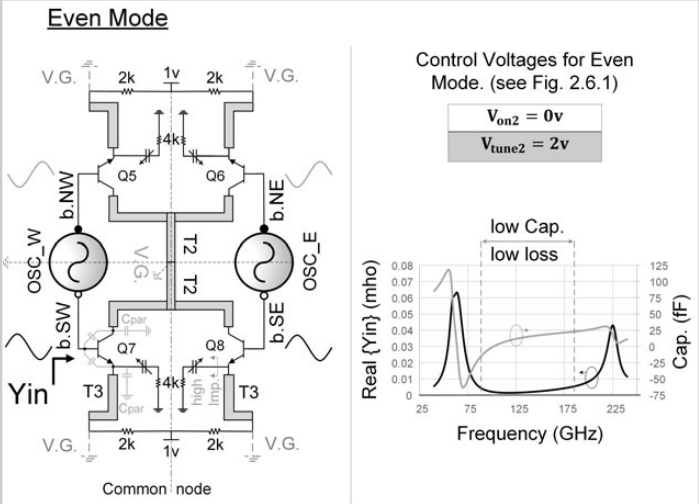


Figure 2.6.2: Even mode of the VCO with the equivalent AMS circuit (left). Simulated input admittance and capacitance of the AMS blocks in even mode (right).

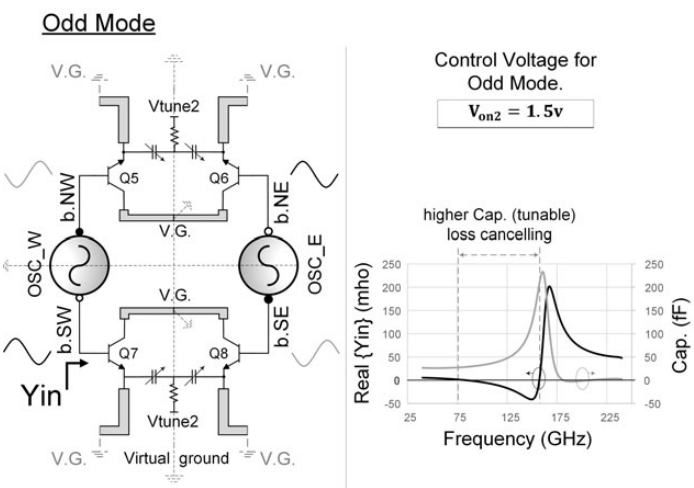


Figure 2.6.3: Odd mode of the VCO and with the equivalent AMS circuit (left). Simulated input admittance and capacitance of the AMS blocks in odd mode for Vtune2 = 2V (right).

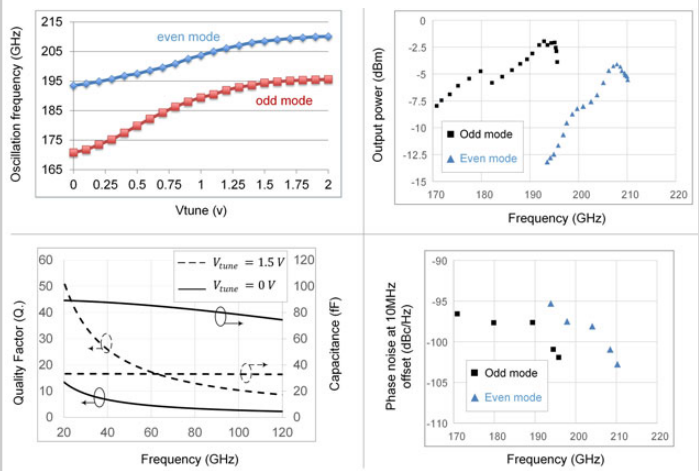


Figure 2.6.4: Measured tuning range vs. Vtune (upper-left). Measured power vs. frequency (upper-right). Simulated capacitance and quality factor of the varactors vs. frequency (lower-left). Measured phase noise vs. frequency (lower-right).

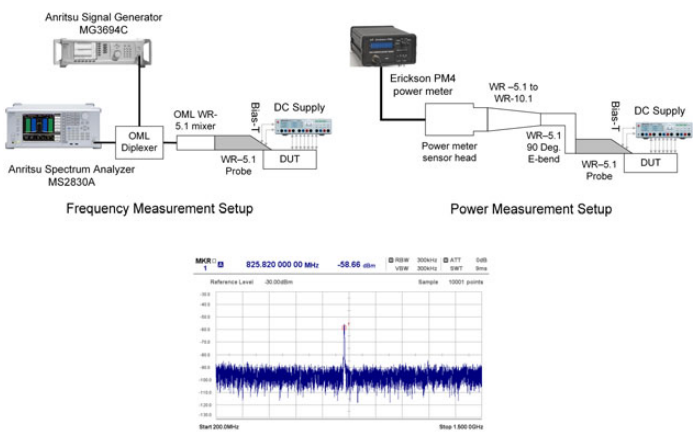


Figure 2.6.5: Measurement setup (top). Spectrum analyzer output for 210.1GHz output (bottom).

Reference	[1]	[2]	[3]	[4]	[6]	[7]	This Work
Center Freq. (GHz)	106.7	256	290	239	260	290	**190.5**
Tuning Range (%)	39.4	4.3 (6.5*)	4.5	12.5	1.4 (9.5**)	8	**20.7**
Fundamental Freq. (GHz)	26.7	128	72.5	119.5	130	96.7	**95.25**
Max. Output Power (dBm)	-15	4.1	-1.2	-4.8	0.5	-14	**-2.1**
Max. DC Power (mw)	45	227	325	18.5	800	105.6	**294 (Odd mode) 183 (even mode)**
Best Phase Noise (dBc/Hz)	-108.2 @10MHz	-94 @1MHz	-78 @1MHz	-110.9 @10MHz	-78 @1MHz	-80.28 @1MHz	**-102.64 @10MHz**
Technology, f_{max} (GHz)	65nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS	90nm BiCMOS 315GHz	**130nm BiCMOS 210GHz**
Measurement	Probing	Probing	Probing	Probing	Radiation	Probing	**Probing**

* Including frequency tuning by change of supply voltage.

** Pulse modulation for broadband radiation. Not continuous frequency tuning.

Figure 2.6.6: Comparison table with prior works.

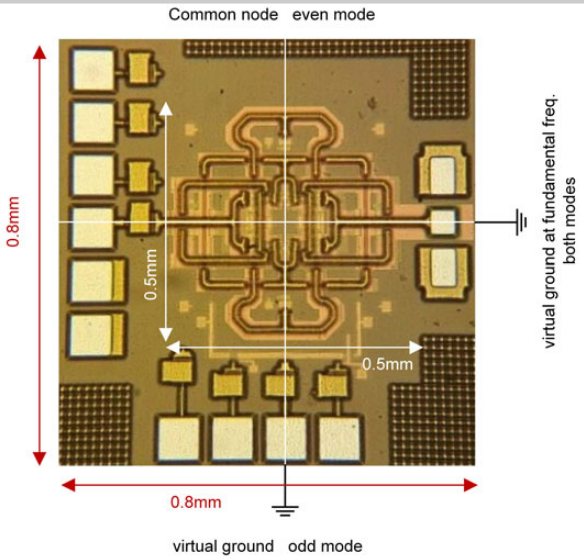


Figure 2.6.7: Die micrograph.

978-1-4673-9467-3/16/$31.00 ©2016 IEEE

2.7 A 0.003mm² 1.7-to-3.5GHz Dual-Mode Time-Interleaved Ring-VCO Achieving 90-to-150kHz 1/f³ Phase-Noise Corner

Jun Yin[1], Pui-In Mak[1], Franco Maloberti[2], Rui P. Martins[1,3]

[1]University of Macau, Macau, China, [2]University of Pavia, Pavia, Italy, [3]Instituto Superior Tecnico, Lisbon, Portugal

Ring-VCOs (RVCOs) [1] have been avoided for over a decade for high-performance RF systems due to their much lower FOM (<165dB [2]) than that of their LC counterparts from low to high frequency offsets. Yet, as the cost of ultra-scaled CMOS technologies is escalating, the small-die-area and wide-tuning-range advantages of RVCOs have attracted more attention recently, aiming to break the FOM limit at the system level. In [2], a type-I PLL succeeds in suppressing the RVCO phase noise (PN) by extending the loop bandwidth to 10MHz ($f_{ref}/20 \rightarrow f_{ref}/2$), facilitating an ultra-compact (0.015mm²) frequency synthesizer for 2.4GHz WLAN. However, the type-I PLL only offers 20dB/dec phase-noise suppression for its RVCO. Thus, despite using large transistors (36/0.28μm), the 1/f³ PN corner (f_{1/f^3}) is still high (~4MHz), degrading the overall jitter performance of the PLL. This paper proposes a dual-mode time-interleaved RVCO (TI-RVCO). It offers interesting properties of extending the frequency tuning range and reducing f_{1/f^3} corner (~1MHz → ~100kHz), resulting in a better FOM over a wide range of frequency offsets (10kHz to 1MHz). The achieved f_{1/f^3} noise corner (~90kHz to 150kHz) is comparable to the state-of-the-art LC-VCOs [3, 4].

One effective way to suppress the 1/f³ noise is to avoid the 1/f noise upconversion, which can be predicted by the impulse sensitivity function (ISF) [1]. Since 1/f noises generated by NMOST and PMOST are uncorrelated, their induced PN power spectral densities is added (Fig. 2.7.1a). Assuming a triangular-shape ISF ($|\Gamma| = |\Gamma_{nmos}| = |\Gamma_{pmos}|$) and the same 1/f noise corner ($f_{1/f}$) for both NMOST and PMOST, the f_{1/f^3} of a multi-stage RVCO can be revised from [1] as

$$f_{1/f^3} = f_{1/f} \frac{3}{4\eta} \times \frac{1}{\text{No. of Stage}}$$

where η is a proportionality constant between each stage delay τ and the maximum slope k_{max} of the normalized RVCO output. Thus, given the transistor sizes and supply voltage (V_{DD}), increasing the number of stage helps reducing f_{1/f^3} corner, but at the expense of a lower output frequency.

The proposed TI-RVCO (Fig. 2.7.1b) extends the typical N-stage RVCO to NxM stages (M: the time-interleaved factor), such that all delay stages are relaxed in terms of operating frequency, i.e. f_o/M. A high-frequency output f_o is upheld by properly recombining the internal multi-phase outputs via a time-windowed phase combiner (TWPC). As long as the TWPC adds no noise, the RMS jitter of the combined output signal remains the same as that of a typical NxM-stage RVCO, while the output period is reduced by a factor M. Thus, the phase-noise profile of an NxM-stage TI-RVCO is an M-time-upshifted version of a typical NxM-stage RVCO (Fig. 2.7.1c), while keeping f_{1/f^3} unchanged. As a result, f_{1/f^3} would be reduced by M times when compared with a typical N-stage RVCO directly operating at f_o. The NxM-stage TI-RVCO can achieve the same 1/f² noise at large frequency offsets as the N-stage RVCO, since its 1/f² noise $\propto \Gamma_{rms}^2$ and thus $\propto 1/(NxM)^2$.

Enlarging the M factor can further reduce f_{1/f^3}, but this implies extra phases for combining, which exacerbates both delay mismatches in the TWPC and difficulty of the layout. Also, a large M factor leads to closer output spurs in the vicinity of f_o, i.e. $\pm hf_o/M$ where h=1,2,3... As the typical f_{1/f^3} of a RVCO, in advanced CMOS technologies, is around several MHz, a practical value of M can be 7, which is adequate to reduce f_{1/f^3} to several hundreds of kHz without compromising much on the spur level, power consumption and die area.

The desired phase combiner should be power efficient and should add minimum delay offset and mismatch between the different phases, which otherwise cause deterministic jitter and/or output spurs. The conventional phase combiner used in DLL-based clock multipliers [5] (Fig. 2.7.2a) suffers from a severe delay offset due to the asymmetrical inputs of the OR gate. Here, the proposed TWPC (Fig. 2.7.2b) eliminates fully the delay offset, as each selected phase can pass only through the transmission gate within the time window T_{win}. To ensure all time windows ($S_{5,10,15}$) are non-overlapping, T_{win} is upper-bounded by $(N-2)T_o/(2N)$ with N≥5. Thus, logic gates in the phase selector can be minimally sized to save power since T_{win} is long enough to tolerate reasonable PVT variations and mismatches. From Monte-Carlo (MC) simulations at f_o=3.5GHz (N=5, M=3), the mean and standard deviation, σ, of T_{win} are 87ps and 1ps, respectively. The tolerable time difference (T_p, Fig. 2.7.2b) is 29.7ps (σ=0.78ps), ensuring the rise/fall edge of each phase is captured within T_{win}. Comparatively, the phase combiner in Fig. 2.7.2a has a delay offset of +4/-6.4ps and a delay mismatch of σ=0.39ps, while the proposed circuit reduces the delay mismatch by 3.25× to σ=0.12ps and achieves a negligible delay offset (+10/-8fs) under a 0.1mW power budget.

To extend the tuning range, the TI-RVCO (Fig. 2.7.3) features a reconfigurable factor M. The selection of M depends on the original tuning range (TR_o) of the NxM-stage RVCO. If M is selectable as M_1 or M_2 (M_2>M_1), TR_o should be larger than $2(M_2-M_1)/(M_2+M_1)$ to allow a certain overlap between the 2 output bands. Under M=5 or 7, the output tuning range at f_o can be roughly doubled (~70%) relative to TR_o (38%). Besides, M≥5 is adequate to reduce the f_{1/f^3} corner from 1MHz to ≤200kHz. Such a dual-mode operation widens the tuning range using a small V_{DD} range. A very low V_{DD} is unfavorable as it significantly degrades the PN due to limited current and voltage swings. Dominated by the device mismatch in the delay stages, the output period at 3.5GHz shows a mismatch of σ=0.8ps (0.3% of T_{out}) in schematic-level MC simulations, resulting in output spurs <-50dBc.

Three prototypes were fabricated in 65nm CMOS (Fig. 2.7.7) for comparison: a 35-stage dual-mode TI-RVCO, a 15-stage TI-RVCO and a typical 5-stage RVCO. All delay stages have the same CMOS inverters (PMOST: 14/0.18μm, NMOST: 7/0.18μm). The f_{1/f^3} corner of the dual-mode TI-RVCO is reduced by 6.2× (930kHz→150kHz) when compared with that of a typical RVCO (Fig. 2.7.4), which follows closely the prediction of 7× by the ISF theory. At ~3.3GHz carrier, f_{1/f^3} corner is 150kHz for the TI-RVCO, which is comparable to the state-of-the-art LC-VCOs [3] (120 to 240kHz) and [4] (60 to 100kHz) that already feature 1/f³-noise-reduction techniques. The output spurs within the frequency offset $f_o \pm 2f_o/7$ are <–43.1dBc at V_{DD}=1V, which are mainly limited by the deterministic mismatch in the 2D layout to balance the dual modes (Fig. 2.7.7), and can likely be resolved by delay compensation in TWPC. The PN and FOM between the dual-mode TI-RVCO and typical RVCO are compared in Figs. 2.7.5a and b. The former achieves better results from 10kHz to 1MHz offsets, and shows a 68.5% tuning range using only 30% of V_{DD} downscaling (1 to 0.7V) with an adequate overlap (130MHz) between the two modes. The power efficiency is ~0.5mW/GHz at 3GHz (Fig. 2.7.5c), which is ~1.5× of the 5-stage RVCO.

Benchmarking with a typical 5-stage RVCO (Fig. 2.7.6), the dual-mode TI-RVCO reduces the f_{1/f^3} by 6.2×, which results in an improvement of FoM@10kHz/100kHz/1MHz by 6.8/4.5/0.7dB, respectively. Likewise, when contrasted with the RVCO + N-path filter technique [6], our TI-RVCO achieves >40× lower f_{1/f^3}, 10dB better FoM@100kHz offset and 5× smaller die area. The TI-RVCO, inherently offering a div-by-M output and can benefit the type-I PLL [2] in terms of power and PN over a wide range of frequency offsets, resulting in a better overall jitter performance.

Acknowledgements:
The authors thank Macao FDCT and MYRG-2015-00097 for financial support.

References:

[1] A. Hajimiri et al., "Jitter and Phase Noise in Ring Oscillators," *IEEE J. Solid-State Circuits,* vol. 34, no. 6, pp. 790-804, June 1999.
[2] L. Kong and B. Razavi, "A 2.4GHz 4mW Inductorless RF Synthesizer," *ISSCC Dig. Tech. Papers*, pp. 450-451, Feb. 2015.
[3] D. Murphy et al., "A VCO with Implicit Common-Mode Resonance," *ISSCC Dig. Tech. Papers*, pp. 442-443, Feb. 2015.
[4] M. Shahmohammadi et al., "A 1/f Noise Upconversion Reduction Technique Applied to Class-D and Class-F Oscillators," *ISSCC Dig. Tech. Papers*, pp. 444-445, Feb. 2015.
[5] D. Foley and M. P. Flynn, "CMOS DLL-Based 2-V 3.2-ps Jitter 1-GHz Clock Synthesizer and Temperature-Compensated Tunable Oscillator," *IEEE J. Solid-State Circuits,* vol. 36, no. 3, pp. 417-423, Mar. 2001.
[6] C. Zhai et al., "An N-path Filter Enhanced Low Phase Noise Ring VCO," *IEEE Symp. VLSI Circuits*, pp. 234-235, June 2014.

 978-1-4673-9467-3/16/$31.00 ©2016 IEEE

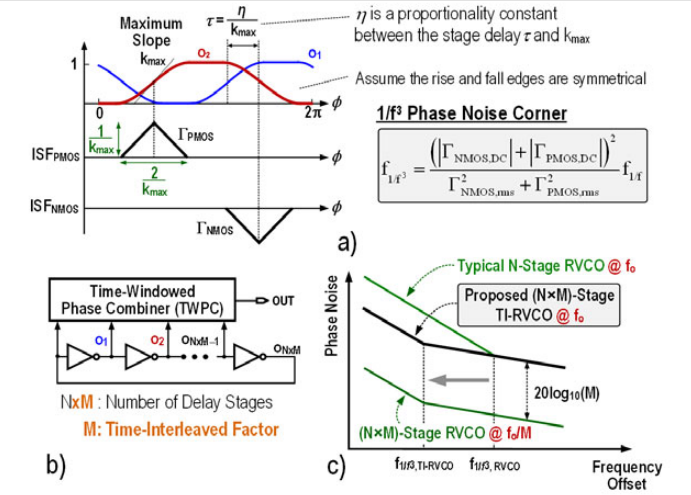


Figure 2.7.1: a) Predicted by the ISF, extending the number of delay stages in a RVCO can reduce the 1/f³ PN; b) TI-RVCO to achieve a smaller 1/f³ PN corner, as shown in c), while keeping a high f_o.

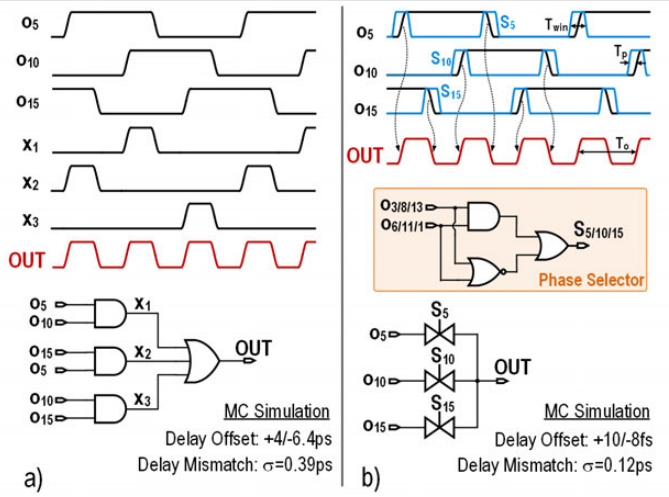


Figure 2.7.2: a) Typical logic-phase combiner [5] suffers from large delay offset and mismatch in the OR gate. b) Proposed TWPC nullifies the delay offset, and has 3.25× lower delay mismatch.

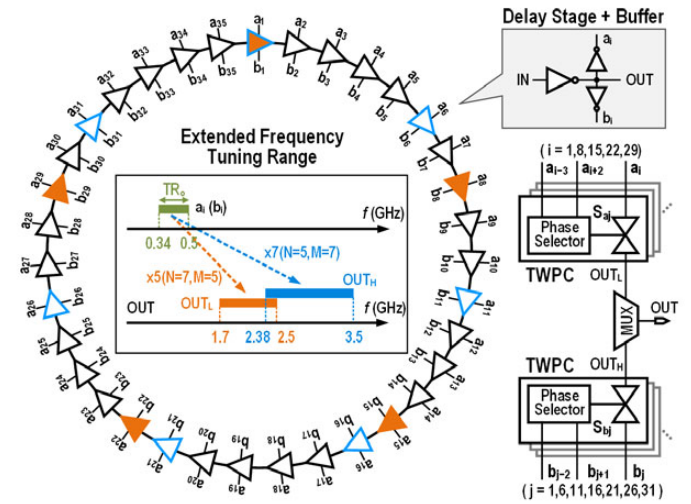


Figure 2.7.3: Proposed 35-stage dual-mode TI-RVCO. By properly combining the different output phases for high-band (×7) and low-band (×5) modes, the frequency tuning range can be extended.

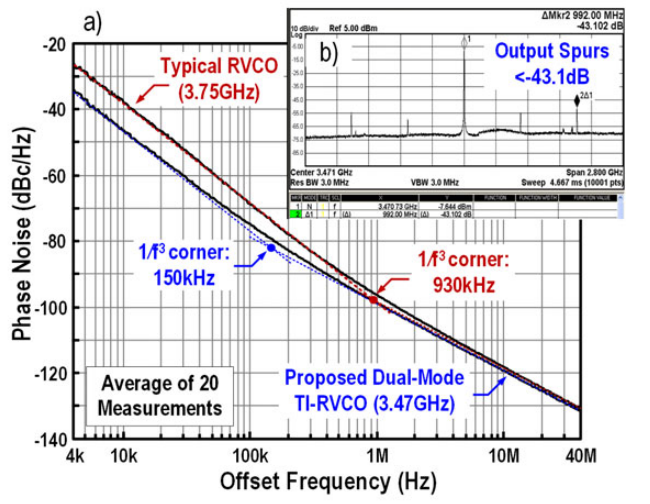


Figure 2.7.4: Measured a) PN of a typical RVCO and the proposed 35-stage dual-mode TI-RVCO; b) Mismatch-induced output spurs of the 35-stage dual-mode TI-RVCO.

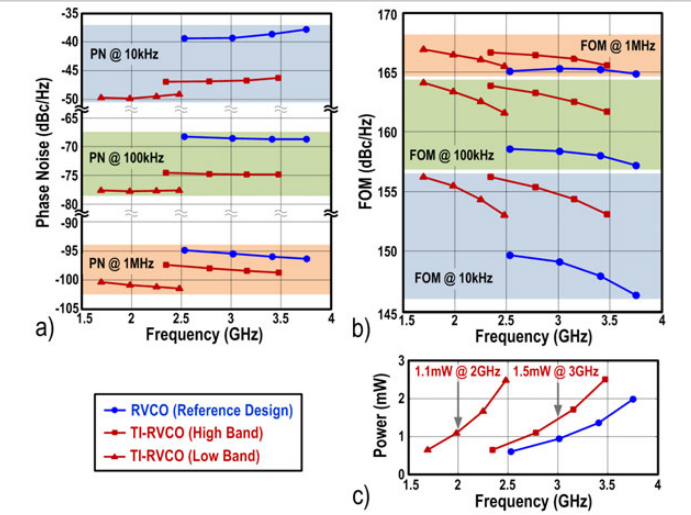


Figure 2.7.5: Measured a) PN; b) FOM; c) power consumption of the typical 5-stage RVCO and the proposed 35-stage dual-mode TI-RVCO in low- and high-band modes.

	3 Prototypes Fabricated in This Work				VLSI'14 [6]
Technique	35-Stage Dual-Mode TI-RVCO		15-Stage TI-RVCO	Typical 5-Stage RVCO	RVCO + N-Path Filter
Frequency Range (GHz)	1.7 to 3.47 (68.5%)		2.35 to 3.41 (36.8%)	2.53 to 3.75 (38.9%)	0.3 to 1.2 (120%)
Carrier (GHz) @V_{DD}	1.7 @ 0.7V	3.47 @ 1V	3.41 @ 1V	3.75 @ 1V	1.0 @ 1.2V
1/f³ Noise Corner (kHz)	90	150	340	930	6000 *
Power (mW)	0.65	2.51	2.25	1.99	4.7
PN @ 10kHz (dBc/Hz)	−49.7	−46.3	−43.7	−37.8	N/A
PN @ 100kHz (dBc/Hz)	−77.6	−74.9	−73.6	−68.7	−80*
PN @ 1MHz (dBc/Hz)	−100.4	−98.7	−98.9	−96.3	−110
FOM @ 10kHz (dBc/Hz)	156.2	153.1	150.8	146.3	N/A
FOM @ 100kHz (dBc/Hz)	164.1	161.7	160.7	157.2	153.3 *
FOM @ 1MHz (dBc/Hz)	166.9	165.6	166.0	164.8	163.3
Core Area (mm²)	0.003		0.00086	0.00024	0.015
CMOS Technology	65nm		65nm	65nm	65nm

* Estimated from PN plot $\quad FoM = -PN + 20\log_{10}(f_o/\Delta f) - 10\log_{10}(P_{DC}/1mW)$

Figure 2.7.6: Performance comparison.

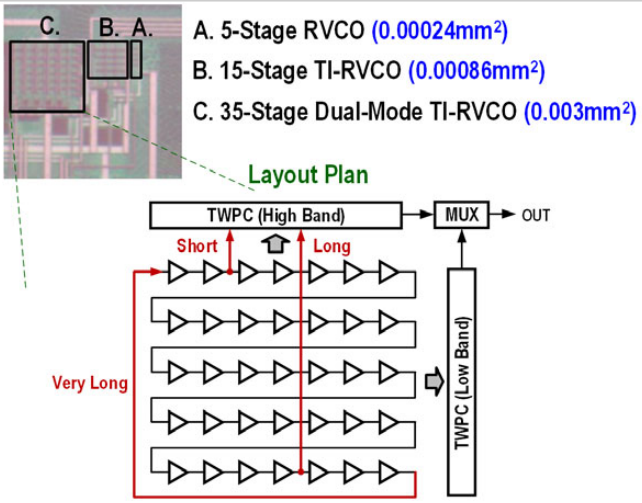


Figure 2.7.7: Die micrograph of the RVCO and TI-RCOs. The 35-stage dual-mode TI-RVCO has 5 rows each having 7 delay stages to be routed to the two TWPCs.

978-1-4673-9467-3/16/$31.00 ©2016 IEEE

2.8 A Mixed-Mode Injection Frequency-Locked Loop for Self-Calibration of Injection Locking Range and Phase Noise in 0.13μm CMOS

Dongseok Shin, Sanjay Raman, Kwang-Jin Koh

Virginia Tech, Blacksburg, VA

Injection-locked oscillators (ILOs) are widely used to realize low-noise carrier sources, particularly at mm-Waves by leveraging harmonic injection, but only within a narrow locking range (Δf_L) [1]. Substantial effort has been made to improve Δf_L by increasing the injection current through multiport injections in open-loop architectures at the expense of a fair amount of extra power dissipation (P_{diss}) [2]. The Δf_L-limitation can also be mitigated by calibrating the free-running frequency (f_{osc}) of the ILO using a mixer-based closed-loop configuration, but at the expense of significant hardware complexity in the multi-frequency feedback control and substantially increased P_{diss} [3]. In the closed-loop self-calibration technique presented in this paper, the feedback signal is primarily processed in the digital domain after extracting the envelope signal bearing the frequency difference between the injection source (f_{inj}) and f_{osc} in the analog domain, resulting in a compact and power-efficient injection-frequency locked loop (IFLL) tracking the 3rd-harmonic of f_{inj} over 26.5-to-29.7GHz (Δf_L: 11.4%) with a 2.4mW P_{diss} in the calibration circuits.

Figure 2.8.1a shows the mixed-mode IFLL architecture for a Δf_L calibration of the quadrature ILO (QILO). The QVCO (Fig. 2.8.2a), employing both super-harmonic inductive coupling at the tail [4] and symmetric in-phase coupling at the load [5] for better phase noise (PN) with less I/Q phase error, injects a 8.8-to-10GHz (f_{inj}) signal to the QILO (Fig. 2.8.2b) comprised of LC tanks with 5b switched-C array and coupling transconductors. The QILO utilizes the 3rd-harmonic of the injection current to establish frequency locking, typically < 3% of Δf_L due to a relatively small 3rd-harmonic power compared with the fundamental power. The calibration of Δf_L primarily relies on the frequency detection or FM-to-AM conversion capability of the QILO [6]. When $3f_{inj}$ deviates beyond the intrinsic Δf_L from the QILO free-running frequency, the QILO starts to lose lock and produces an AM and PM modulated signal, of which the AM modulation frequency (f_{AM}) is proportional to $\{(f_{osc}-3f_{inj})^2-(\Delta f_L/2)^2\}^{1/2}$ [1]. In the IFLL, the AM modulated signal is demodulated in Fig. 2.8.1 using the envelope detector, comprised of source followers and load capacitor C_{ED} in Fig. 2.8.2c, followed by rail-to-rail amplification through the 5-stage feedback-inverter amplifier chain to generate pulse signal. To prevent false pulses due to DC or low-frequency noise, the overall gain in the limiting amplifiers is bandpass shaped by leveraging node poles and zeros created by transistor parasitics, C_{ED}, C_b and R_f. In simulations, the minimum detectable frequency ($f_{AM,MIN}$) is around 60MHz, corresponding to a ~20dB gain crossing point in the gain response shown in Fig. 2.8.2c.

The pulse signal is then fed to both an 8b shift register (SR) and update-controller in Fig. 2.8.1 to be processed further in digital domain. The digital processing creates a feedback signal that controls the amount of capacitance in the switched-C array such that the QILO can track the injection frequency, calibrating Δf_L and limiting Δf_L to the tuning range of the QILO. When unlocked, the SR and the AND gate produce pulses after counting 8 consecutive pulses and drive the charge (Q) pump that discharges C_I (2pF) progressively toward enabling the upper path of the update-controller. Consequently, the 5b counter increases the LC-tank capacitance by 1LSB capacitance (ΔC) in the switched-C array, decreasing the QILO f_{osc} by Δf due to the ΔC change. When locked, the Q-pump charges the integrator C_I toward logic-high disabling the update path. When locked at the edge of the Δf_L, the QILO PN degradation is significant. Thus, as a final step in the calibration, at the moment the Q-pump output (Fig. 2.8.1④) becomes high, the lower path in the update-controller creates a further pulse to increase the LC tank capacitance by 1-LSB ΔC, pushing the frequency toward the center of the locking range and thus preventing the PN degradation as illustrated in Fig. 2.8.1b. To ensure PN calibration, the amount of frequency shift from the edges to the center of Δf_L is approximately 20% of the Δf_L. Therefore, the frequency resolution (Δf), corresponding to a 1LSB ΔC update, needs to satisfy $f_{AM,MIN}+0.2\Delta f_L \leq \Delta f \leq 1/2(f_{AM,MIN}+0.8\Delta f_L)$.

Figure 2.8.3 shows typical transient simulation results at each designated node of the IFLL in Fig. 2.8.1a for the case of QVCO f_{inj}=9.43GHz and QILO initially free-running at f_{osc}=30.1GHz. The envelope magnitude is a nonlinear function of f_{AM}. Due to the large separation between $3f_{inj}$ and $f_{osc,}$ the QILO is unlocked and the output envelope magnitude is small (<50mV$_{pp}$) at the beginning of the calibration (<20ns) in Figs. 2.8.3① and②. However, the limiter produces rail-to-rail pulses (Fig. 2.8.3③) due to its large gain, >60dB@f_{AM}=1.8GHz, and initiates the Δf_L-calibration, decreasing f_{osc} to 28.3GHz ($3f_{inj}$) progressively in a nonlinear fashion as the switched-C array code being updated every 8 clock cycle of the f_{AM} in Fig. 2.8.3⑤. When f_{osc} approaches the edge of Δf_L (300MHz) at around 130ns, the AM-modulation effect in the QILO output becomes more pronounced (insert in Fig. 2.8.3①) and after 8 pulses the feedback counter updates the switched-C array code to 01100, locking the QILO to the QVCO at the edge of Δf_L. Subsequently, after locking the Q-pump starts charging C_I creating a lock signal, which pushes one more LSB code up to 01101 at around 175ns in Figs. 2.8.3④ and ⑤, pushing f_{osc} closer to 28.3GHz to calibrate PN in Fig. 2.8.3①. Note that the 8b SR acts as a pulse filter, having 8 consecutive pulses to drive the Q-pump; e.g, bursts of irregular pulses due to a brief transient waveform uncertainty after locking are ignored by the pulse filter.

The proposed IFLL was realized in 0.13μm CMOS and was characterized on-wafer (GSSG probes) by measuring the differential RF signal at the VCO outputs. Since all digital circuits are driven autonomously by the envelope pulse, no external control clock is required. The typical measured PN of the QVCO at 8.84GHz is -117.2dBc/Hz and -129.6dBc/Hz at 1MHz and 10MHz offset, respectively (Fig. 2.8.4a). When the QILO is 3rd-harmonically locked by the QVCO, the PN decrease is consistently ~10.5dB at both 20dB-rolloff and flat regions, resulting in -106.8dBc/Hz and -118.9dBc/Hz PN at 1MHz and 10MHz offsets, respectively, at 26.54GHz in Fig. 2.8.4b. More comprehensive frequency measurement results are shown in Fig. 2.8.5. The measured QVCO PN at 5MHz offset ranges from -130dBc/Hz@8.8GHz to -115dBc/Hz@9.9GHz (Fig. 2.8.5①). With the IFLL disabled and by decreasing the QVCO f_{inj} from 9.9GHz to 9.8GHz, the QILO can maintain lock from 29.7 to 29.4GHz (Δf_L=300MHz, QILO free-running f_{osc} is 29.55GHz) but the PN degrades by 18-to-20.5dB at the edges of the Δf_L from the minimum of -107.5dBc/Hz (Fig. 2.8.5②). Thus, a more effective locking range, with only 10-to-10.5dB PN degradation from the QVCO PN, is from 29.48 to 29.66GHz (180MHz), 60% of Δf_L as shown in Figs. 2.8.5③ and ④. When the IFLL is enabled, the QILO can track the QVCO injection frequencies and exhibits consistent 9-to-10dB PN degradation with ±1dB error for the entire measurement range of 26.4-to-29.7GHz (Fig. 2.8.5③). The QVCO and QILO consume 14.4mW and 20.8mW of power, respectively. The P_{diss} in the calibration circuits, excluding the QILO, is 2.4mW, >27× smaller than in [3], while achieving equivalent locking range (11.4%, Table I in Fig. 2.8.6). The QILO PN performance is on par with other designs in Fig. 2.8.6 when the frequency scaled to a similar range (Table II). The chip size is 1×1mm^2 including pads, while the area penalty due to the auxiliary calibration circuits is negligible (Fig. 2.8.7).

Acknowledgements:
This work was supported in part by the Ministry of Trade, Industry and Energy (MOTIE) grant funded by the Korean government (No. 10050527).

References:

[1] B. Razavi, "A Study of Injection Locking and Pulling in Oscillators," *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1415–1424, Sept. 2004.

[2] A. Musa et al., "A Low Phase Noise Quadrature Injection-Locked Frequency Synthesizer for MM-Wave Applications," *IEEE J. Solid-State Circuits*, vol. 46, no. 11, pp. 2635–2649, Nov. 2011.

[3] W. Deng et al., "A Sub-Harmonic Injection-Locked Quadrature Frequency Synthesizer with Frequency Calibration Scheme for Millimeter-Wave TDD Transceivers," *IEEE J. Solid-State Circuits*, vol. 48, no. 7, pp. 1710-1720, July 2013.

[4] S. Gierkink et al., "A Low-Phase-Noise 5-GHz CMOS Quadrature VCO Using Superharmonic Coupling," *IEEE J. Solid-State Circuits*, vol. 38, no. 7, pp. 1148-1154, July 2003.

[5] X. Yi et al., "A 57.9-to-68.3 GHz 24.6 mW Frequency Synthesizer with In-Phase Injection-Coupled QVCO in 65 nm CMOS Technology," *IEEE J. Solid-State Circuits*, vol. 49, no. 2, pp. 347–359, Feb. 2014.

[6] J. Bae et al., "A Low Energy Injection-Locked FSK Transceiver with Frequency-to-Amplitude Conversion for Body Sensor Applications," *IEEE J. Solid-State Circuits*, vol. 46, no. 4, pp. 928–937, Apr. 2011.

 978-1-4673-9467-3/16/$31.00 ©2016 IEEE

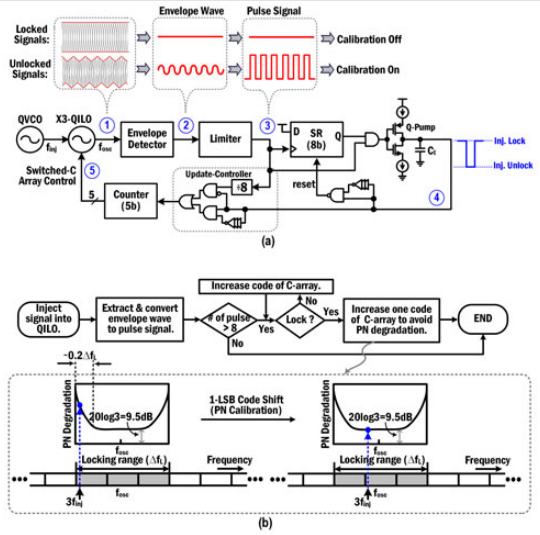


Figure 2.8.1: (a) Block diagram of the IFLL and (b) flowchart for frequency calibration followed by phase-noise calibration.

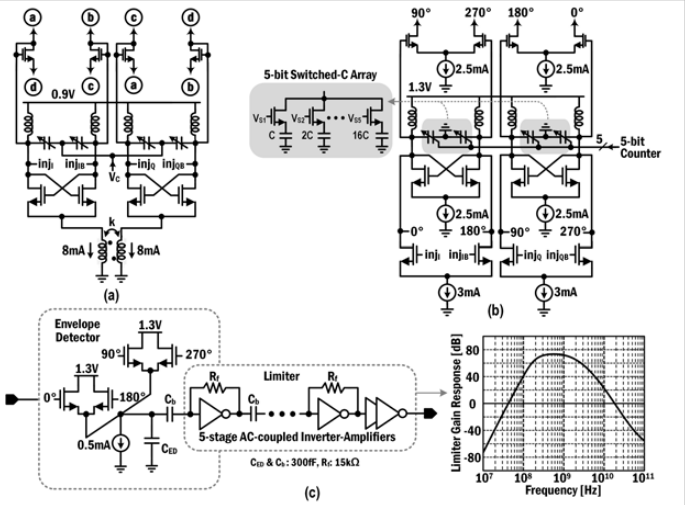


Figure 2.8.2: Schematics of (a) QVCO, (b) QILO, and (c) an envelope detector cascaded with feedback-inverter-based limiting amplifiers and the gain response.

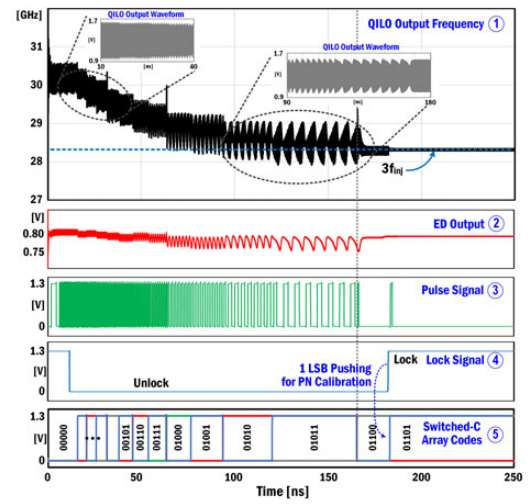


Figure 2.8.3: SPECTRE transient simulation results at each corresponding node designated in Fig. 2.8.1: QVCO f_{inj}=9.43GHz and QILO initial free-running f_{osc}=30.1GHz.

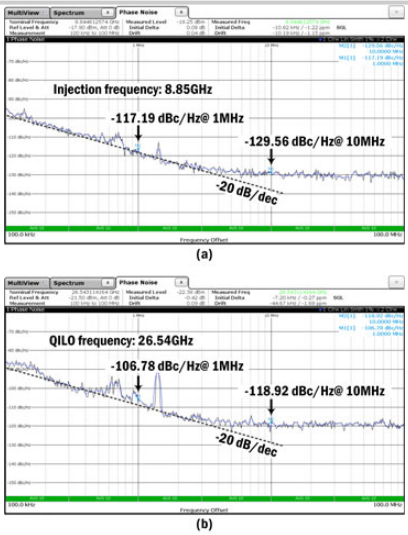


Figure 2.8.4: Measured phase noise spectrum: (a) QVCO (f_{inj}=8.85GHz) and (b) QILO when locked to 3rd-harmonic of the QVCO.

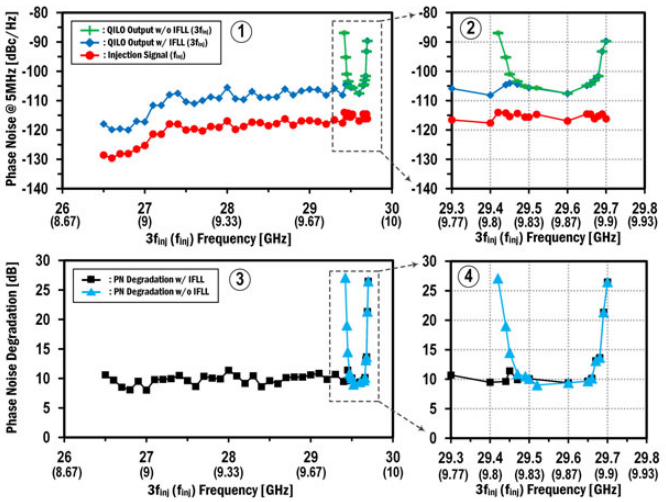


Figure 2.8.5: Measured QVCO phase noise vs frequency and QILO phase noise with and without enabling the IFLL (①&②), and the phase noise degradation in the QILO with and without enabling the IFLL (③&④).

Table I. Calibration circuit comparison

	W. Deng JSSC13 [3]	This Work
Tech	65nm CMOS	130nm CMOS
Feature	PLL+Mixer +Doulber	Envelope Detector
Locking Range (%) (w/o Calibration)	11.2 (0.5)	11.4 (1)
VDD (V)	1.2	1.3
Power (mW)	65	2.4
Area (mm²)	~ 0.95*	0.015
Locking Time	< 42.7us	< **300ns
Operation	Externally Controlled	Autonomous

*Estimation based on chip photograph.
**Estimation based on simulations.

Table II. Comparison with prior state-of-the-art works

	Q. Wu ISSCC13	A. Musa JSSC11 [2]	W. Deng JSSC13 [3]	This Work
Tech	130nm SiGe	65nm CMOS	65nm CMOS	130nm CMOS
Phase	Diff.	Quad.	Quad.	Quad.
Frequency (GHz)	27.9 -37.8	67.2-67.7	58.1-65	26.5 -29.7
VDD (V)	1.5	1.2	1.2	1.3
Power (mW)	10 (VCO only)	68	137	*38.6 (**49.7)
Phase Noise (dBc/Hz@1MHz offset)	-103.6 @32.9GHz	-95 @60GHz	-96 @61.5GHz	-106.8 @26.5GHz
Chip Area (mm²)	1.93	0.8 (QILO only)	3.8	1
Feature	BiCMOS Cross-coupled Pair VCO	PLL+QILO w/ Dual Injection	PLL+QILO + Calibration Circuit	QVCO+QILO + Calibration Circuit

*Without VCO output buffers.
**With including VCO output buffers for measurement with 50-Ω instruments.

Figure 2.8.6: Performance summary and comparison with VCOs and locking range calibration circuits.

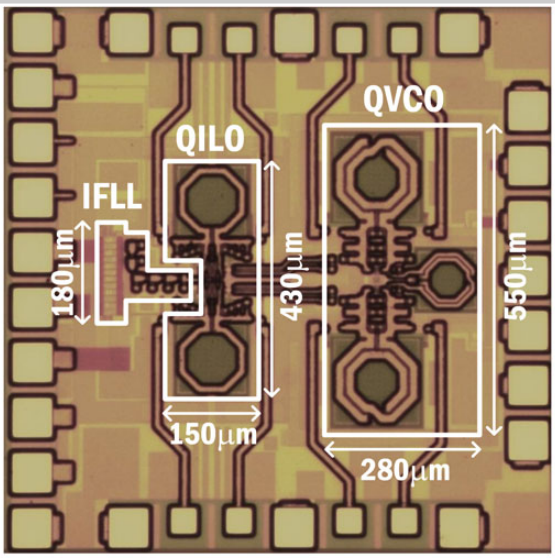


Figure 2.8.7: Die micrograph. Die size: 1x1mm² including pads.

978-1-4673-9467-3/16/$31.00 ©2016 IEEE

2.9 A 2GHz 244fs-Resolution 1.2ps-Peak-INL Edge-Interpolator-Based Digital-to-Time Converter in 28nm CMOS

Sebastian Sievert[1], Ofir Degani[2], Assaf Ben-Bassat[2], Rotem Banin[2], Ashoke Ravi[3], Bernd-Ulrich Klepser[1], Zdravko Boos[1], Doris Schmitt-Landsiedel[4]

[1]Intel, Neubiberg, Germany, [2]Intel, Haifa, Israel, [3]Intel, Hillsboro, OR, [4]Technische Universität München, Munich, Germany

Digital-to-time converters (DTC) generate a clock with a time delay (or phase shift) based on a digital input code. They can be used in clock-and-data-recovery (CDR) circuits [1,2], in the feedback or reference path of a phase-locked loop (PLL) [3,4] or as direct phase modulators in outphasing transmitters (OT) [5]. While DTCs in PLLs often operate close to the reference oscillator frequency, CDR and OT DTCs are required to operate at frequencies in the GHz range. DTCs are often built using a multistage segmented architecture, employing separate coarse and fine delay tuning.

Coarse tuning is usually implemented using multiphase generators based on delay-locked loops (DLLs) [5] or dividers [1], followed by a multiplexer (MUX). Compared to DLLs, dividers do not require a control loop and can achieve lower jitter, but their input clock frequency has to be a multiple of the output frequency. The fine tuning is commonly implemented either with delay cells [4,5], which tune the RC constant of a node to modify the signal zero crossing time, or with phase interpolators (PI) [1]. While delay cells offer high linearity, they cause unwanted supply modulation through a code-dependent current consumption, high jitter through the degradation of the (dis)charge slopes, and do not provide a well-defined delay range. Replica paths with inverted codes are necessary to equalize the current consumption over code [4] and calibration engines are used to cope with the undefined range [5]. PIs on the other hand can provide a full and exact 2π coverage, but have intrinsically high nonlinearity [1,2,6], caused mainly by (a) the ratio $\Delta t/\tau_{int}$ of temporal spacing of the two input signals Δt and the time constant at the interpolation node τ_{int} [2,6] and (b) contention between different interpolation cells (INTC), which leads to short-circuit (cross) currents between V_{DD} and V_{SS} during the interpolation [6]. Harmonic rejection filtering has been introduced to improve the PI linearity [1], but at expense of a lower slew rate of the internal signals and hence jitter.

To achieve a wide range (500ps) with fine resolution (244fs), a full and exact 2π coverage, low jitter and high linearity, this paper presents a DTC incorporating: (a) a multi-modulus-divider (MMD) coarse-tuning stage for 2π coverage, (b) re-sampling of the coarse stage by rising and falling edges of the input clock for low-jitter, (c) a PI-based fine-tuning stage for correct-by-construction coverage, (d) embedding additional logic inside the INTCs to break the contention cross-currents for high linearity. The current consumption of the DTC is equal over all codes, resulting in lower sensitivity to the power supply impedance and avoiding replica paths.

Figure 2.9.1 shows the DTC architecture. It is segmented into 3 stages, that produce successively finer time resolution: in an ultra-coarse tuning stage, an MMD with a 3b resolution produces 2 output signals at 2GHz spaced by $\Delta t_{uc} = T_{out}/8 = 62.5$ps, a coarse-tuning stage reduces this spacing with a 1b resolution to $\Delta t_c = 31.25$ps, and a fine-tuning stage interpolates with a 7b resolution between the 2 coarse tuning outputs with a time resolution of 244fs.

The MMD divider core produces two 2GHz output signals from an 8GHz voltage controlled oscillator (VCO) signal provided by a PLL, having a nominal division ratio of 4. $MMD_{out,1}$ is aligned with a rising edge of the VCO_P signal, whereas $MMD_{out,2}$ is, depending on n_8, aligned with the rising edge of VCO_N either directly leading or lagging VCO_P of $MMD_{out,1}$. This enables a temporal spacing of $\Delta t_{uc} = T_{VCO}/2 = 62.5$ps between $MMD_{out,1/2}$. The upper 2b ($n_{10:9}$) can re-align $MMD_{out,1}$ with a different rising edge of VCO_P by changing the instantaneous division ratio to 3 or 5 for a single output cycle. This leads to the enclosure of the full 2GHz 2π range by $MMD_{out,1/2}$ over code. The outputs of the MMD core are then re-sampled by low noise flip-flops for low jitter.

The coarse-tuning stage reduces the spacing Δt_{uc} with a 1b resolution to $\Delta t_c = \Delta t_{uc}/2 = 31.25$ps. It has a 2b interface, using n_8 from the MMD to determine whether $MMD_{out,1}$ is leading or lagging $MMD_{out,2}$. The upper of both paths, called MUX path, selects with a MUX (controlled by n_7) either $MMD_{out,1}$ or $MMD_{out,2}$ for output MUX_{out}. The second path, called DEL path and controlled by n_8, selects automatically the "earlier" of $MMD_{out,1/2}$ for DEL_{out}. The delay element in this path delays the signal ideally by 31.25ps. As the delay varies over PVT, it has an additional 5b configuration input $cfg_{4:0}$ to adjust it. The waveforms in Fig. 2.9.1 show the outputs of this stage, depending on the input bits. Through a reduction of Δt, and with this $\Delta t/\tau_{int}$, by 50% at the PI input, the interpolation is linearized significantly [2,6].

After the coarse-tuning stage a PI generates an output signal with a phase enclosed between MUX_{out} and DEL_{out}. The PI is implemented as contention-free digitally controlled edge interpolator (CF-DCEI), which is an inverter-based PI structure as discussed in [1,2,6], interpolating digital edges without additional RC for slewing. The solution implements additional logic to prevent shoot-through current during interpolation, leading to a linearized behavior.

Figure 2.9.2 shows the architecture of the CF-DCEI. The 7b resolution is achieved by placing 128 unit INTCs in an array, and thermometric control ensures a monotonic behavior. All INTCs get identical input signals In_1 and In_2, and their outputs are shorted at the interpolation node V_{int}. Each cell can either be selected to weight In_1 or In_2 in the interpolation process. The INTC core structure is a MUX, based on two tristate inverters. Figure 2.9.3 illustrates the selection of the interpolation cell branches and how the interpolation and selection changes are triggered. Each PMOS and NMOS branch has its own selection signal S_1-S_4. Only one branch per cell can be active, preventing cross currents between V_{DD} and V_{SS} during the time when In_1 and In_2 have different logic levels, which is the key improvement over MUX-like control. This architecture enables interpolation on rising and falling edges, leaving the duty cycle at 50%.

CF-DCEI cells with this logic would leave V_{int} floating between interpolations. Therefore, 16 retention cells (RETC) are introduced, which act as keepers of V_{int} during this period. The design is similar to the INTCs, only the select signals R_1-R_4 are different. n_7 of the coarse-tuning stage indicates whether In_1 is leading or lagging In_2 by Δt_c and is used to select the "earlier" input. Figure 2.9.3 shows the timing diagram of the RETCs. Only one retention branch is active, activated by V_{int} after interpolation and deactivated by the first CF-DCEI input, preventing cross-currents between INTCs and RETCs. Figure 2.9.4 shows simulations of the interpolation process, illustrating retention and interpolation periods.

The DTC has been implemented in 28nm CMOS and occupies an area of 0.009mm². For all measurements the chip internal PLL at 8GHz was used for DTC input clocking. Figure 2.9.5 shows the DTC performance for an ideal delay element configuration, resulting from an external measurement. The transfer function of code n vs. output phase shows the coverage of the full 2π range. As the MMD aligns the circuit periodically with different VCO edges every 512 codes, the nonlinearity is repetitive in this range. The DNL is ≥-63fs (-0.26LSB), meaning a fully monotonic DTC. Spikes of ~300fs (1.25LSB) are visible at multiples of code 256, which toggles the MMD. The INL has a peak value of 1.2ps. The close-in phase noise is dominated by the PLL, and the far-out noise floor at a 100MHz offset is -159dBc/Hz. The simulated current consumption of the MMD, MUX+DEL and CF-DCEI from a 1.1V supply is 5mA, 2mA and 11mA, respectively. The measured current consumption from a 1.4V supply is 18mA. Figure 2.9.6 compares the DTC to recently published designs and Fig. 2.9.7 shows a die micrograph highlighting the DTC blocks and the LDO.

Acknowledgements:
The authors would like to thank N. Alomari, T. Bauernfeind, T. Maletz, Y. Palaskas, S. Pellerano, P. Preyler, M. Schimper, and W. Thomann.

References:
[1] M.-S. Chen et al., "A 0.1–1.5 GHz 8-bit Inverter-Based Digital-to-Phase Converter Using Harmonic Rejection," *IEEE J. Solid-State Circuits*, vol. 48, no. 11, pp. 2681-2692, Nov. 2013.
[2] P. Hanumolu et al., "A Sub-Picosecond Resolution 0.5–1.5 GHz Digital-to-Phase Converter," *IEEE J. Solid-State Circuits*, vol. 43, no. 2, pp. 414-424, Feb. 2008.
[3] J. Ru et al., "A High-Linearity Digital-to-Time Converter Technique: Constant-Slope Charging," *IEEE J. Solid-State Circuits*, vol. 50, no .6, pp. 1412-1423, June 2015.
[4] N. Markulic et al., "A 10-bit, 550-fs step Digital-to-Time Converter in 28nm CMOS", *European Solid State Circuits Conf.*, pp. 79-82, Sept. 2014.
[5] A. Ravi et al., "A 2.4-GHz 20–40-MHz Channel WLAN Digital Outphasing Transmitter Utilizing a Delay-Based Wideband Phase Modulator in 32-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 3184-3196, Dec. 2012.
[6] D. Weinlader, "Precision CMOS Receivers for VLSI Testing Applications", Ph.D. dissertation, Dept. Elect. Eng., Stanford Univ., Stanford, CA, 2001.

 978-1-4673-9467-3/16/$31.00 ©2016 IEEE

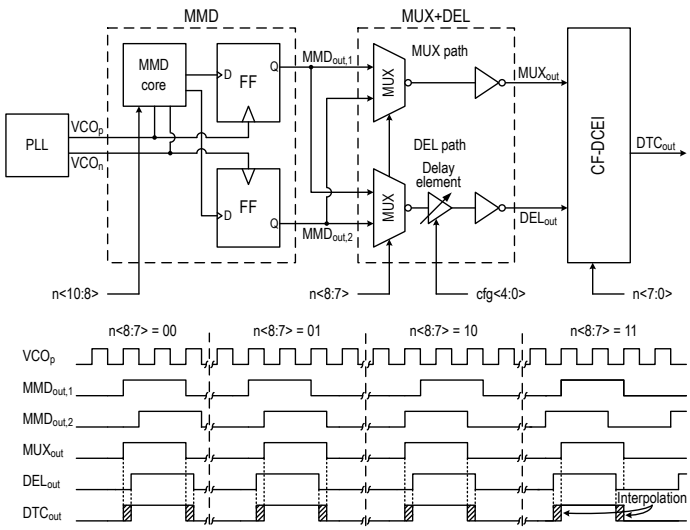


Figure 2.9.1: DTC top block diagram and waveforms.

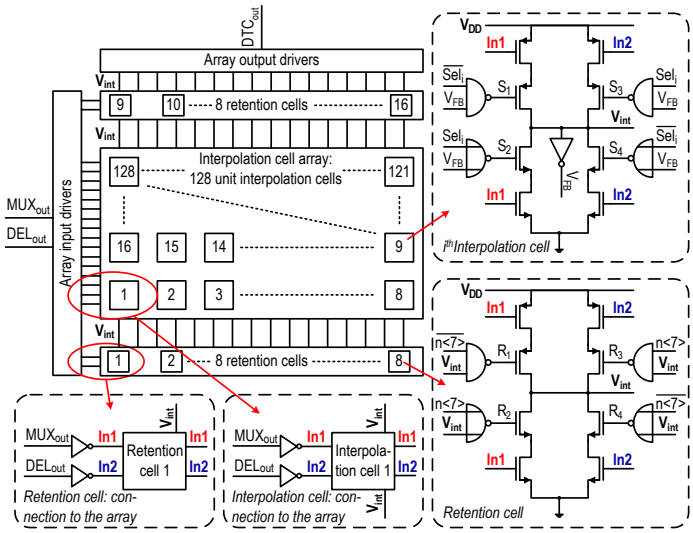


Figure 2.9.2: CF-DCEI array top schematics and implementation of the two types of cells: (i) interpolation and (ii) retention.

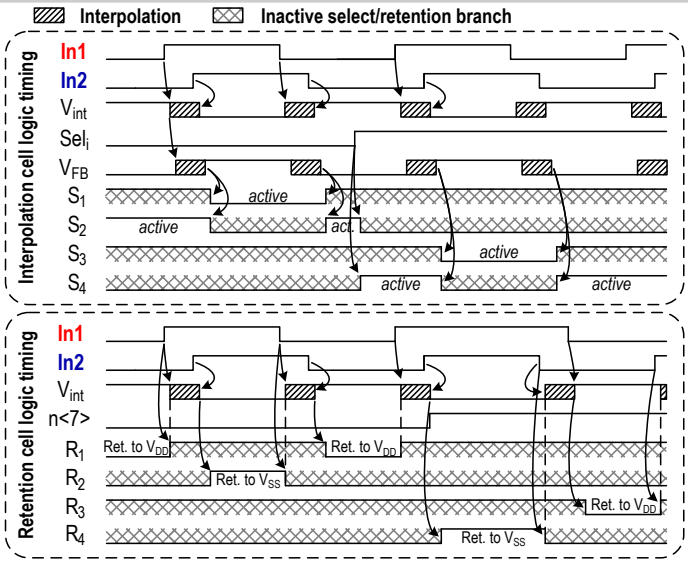


Figure 2.9.3: Logic timing diagram of interpolation and retention cells.

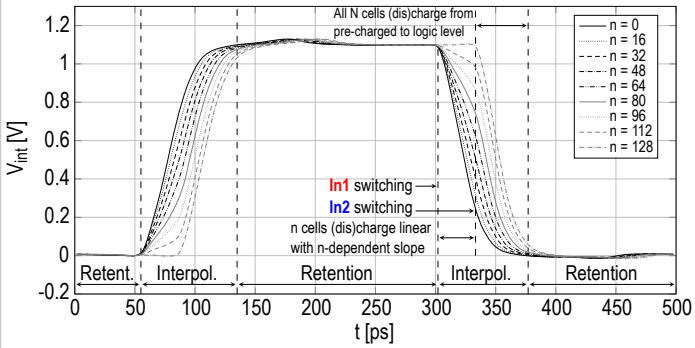


Figure 2.9.4: Simulated CF-DCEI waveforms at the interpolation node V_{int}. The broken contention allows linear (dis)charging of this node when In1 and In2 have different logic levels.

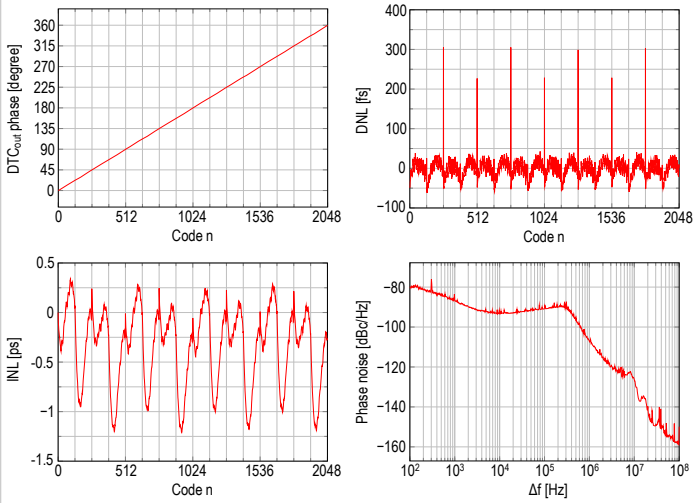


Figure 2.9.5: Measured transfer function, DNL, INL and phase noise.

	This work	JSSC 2013 [1]	JSSC 2012 [5]
Technology	28nm CMOS	65nm CMOS	32nm CMOS
Supply	1.1V	1.2V	1.05V
Frequency	2.0GHz	0.1 –1.5GHz	2.4GHz
Resolution [bit]	11bit	8bit	8bit
Resolution [time]	244fs	2.60 – 39.06ps	1.63ps
Range	2π (500ps) (calibration free)	2π (0.67 - 10ns) (calibration free)	2π (416.67ps) (calibration needed)
DNL (max.)	305fs	4.06ps at 0.5GHz	N/A
INL (max.)	1.2ps	10.4ps at 0.5GHz	2.93ps
Power [mW]	19.8mW	4.3mW at 1.5 GHz	N/A
Area [mm²]	0.009mm²	0.060mm²	0.100mm²

Figure 2.9.6: Comparison table of this work and recently published GHz-domain DTCs.

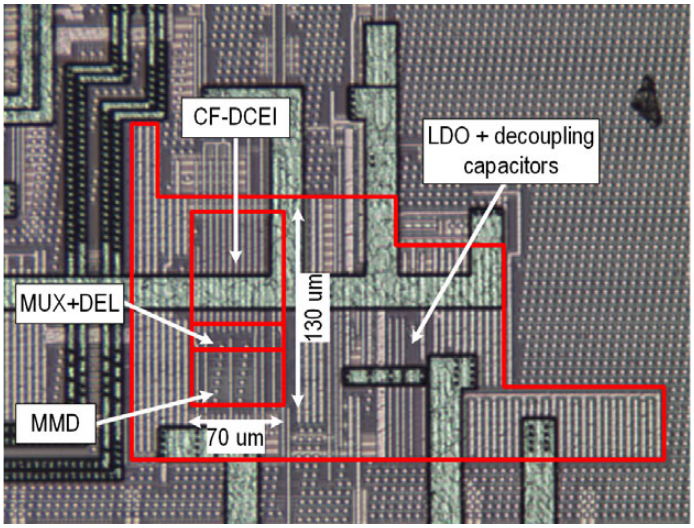


Figure 2.9.7: Die micrograph highlighting single DTC blocks including their LDO.

978-1-4673-9467-3/16/$31.00 ©2016 IEEE